Research Article

Power Management in Low-Power MCUs for Energy IoT Applications

Ling Lin [ID], Zhong Tang, Nianxiong Tan, and Xiaohui Xiao

Vango Technologies, Inc., 310053, China

Correspondence should be addressed to Ling Lin; linling@vangotech.com

In this paper, we identify and address the problems of designing effective power management schemes in low-power MCU design. Firstly, this paper proposes an application-based multipower domain architecture along with a variety of working modes to effectively realize the hierarchical control of power consumption. Furthermore, devices in energy IoT (eIoT) do not always work under the main power supply. When the main power supply is unavailable, the standby power supply (usually the battery) needs to maintain the operation and save the data. In order to ensure the complete isolation between these two power sources, it is always necessary to insert a diode in both select-conduction paths, respectively. In this paper, we built a stable and smooth power switching circuit into the chip, which can effectively avoid the diode voltage loss and reduce the BoM cost. In addition, in the sleep mode, considering the relaxed output voltage range and a limited driving capability requirement, an ultra-low-power standby power circuit is proposed, which can autonomously replace the internal LDO when in sleep, further reducing the sleep power consumption under the main power supply. Fabricated in a standard $0.11\,\mu$m CMOS process, our comparative analysis demonstrates substantial reduction in power consumption from $1\,\mu$A to $0.1\,\mu$A.

1. Introduction

The rapid growth of the energy Internet of Things (eIoT) has driven the vigorous development of microcontrol units (MCUs) [1–3]. In order to provide a lower cost solution, more and more functions are integrated in MCUs: networking, high-efficiency sensor interfaces, etc., which makes the low-power design challenging. Moreover, the application scenarios of eIoT are more complex due to multiple power domains, making low-power design a complex task.

The eIoT is an intelligent system integrating distributed and scalable renewable energy sources and Internet technology with the existing smart grid [4–6]. By controlling the energy flow through the information flow, an overall information transmission and exchange platform is built. The platform connects end users and power supply station, realizing information sharing and transparency and therefore forming an energy ecosystem. The development trend of eIoT is inseparable from the MCU market. Whether it is a small node for connection or a sensor hub for collecting and recording data, it is mainly based on the MCU platform [7, 8].

As the one of the key parts, power management in an MCU for the eIoT is quite challenging [9, 10]. Firstly, the MCU for the eIoT usually has multiple supply domains. For example, apart from the normal supply source, MCUs for smart meters also have a battery supply. Furthermore, the real-time clock (RTC) block is required in the MCU for energy metering. It needs to be working uninterrupted when the meter is in storage or under the power outage. The power dissipation becomes critical for the RTC powered by a battery. Sometimes, the MCU is even required by utility regulations to have a separate RTC power domain. Due to the multiple supply domains, the MCU for eIoT should be compatible with a large supply voltage range of 2.2 V to 5.5 V. Switching among different supply domains with high reliability is also challenging for power management in the MCU. In addition, to extend the battery life, traditional
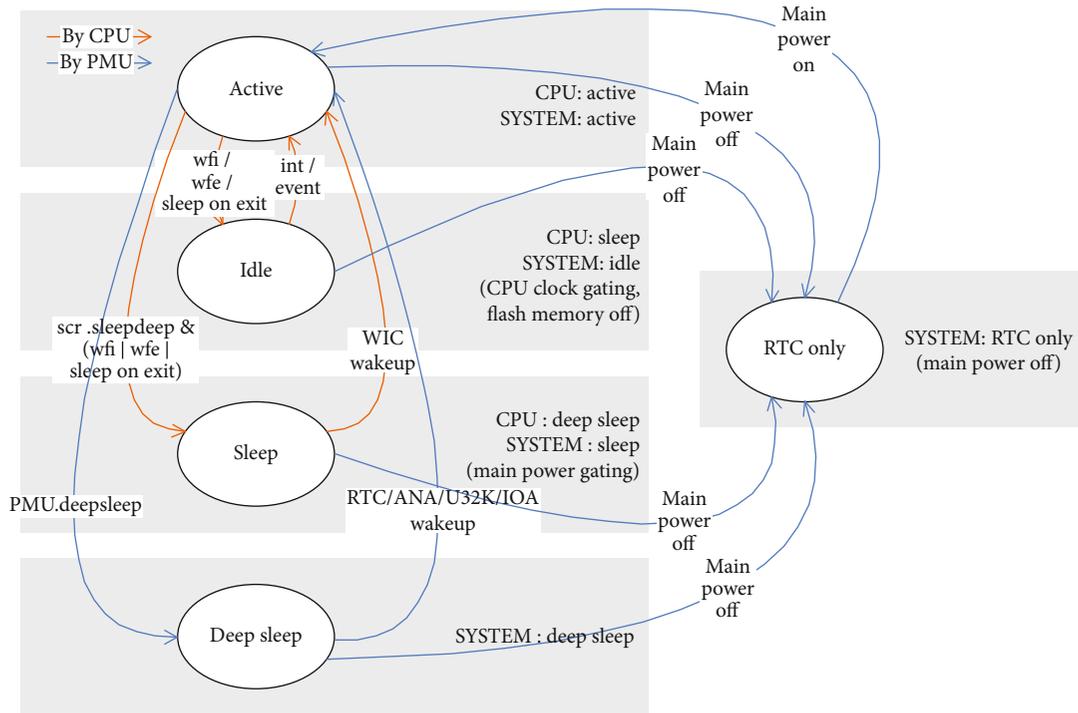
Figure 1: Power state flow chart of the low-power MCU.

techniques such as clock gating and power gating [11] can be used to reduce the power consumption of the digital and analog cores; however, the power consumption of the always-on power management circuits, such as low-dropout regulator (LDO), should be minimized to extend the battery life. At the same time, they should be able to provide a large load current up to 30 mA for the normal working mode.

State-of-the-art ultra-low-power MCUs on the market can achieve submicrowatt power consumption in low-power mode; however, they can only supply a single standard 3.3-V supply voltage [12], which requires additional power switching circuit on-board, increasing the design cost for eIoT applications. As for the LDO in the MCU with large load current as well as low quiescent current, a digitally adaptive LDO scheme is proposed in [13]; however, the driving ability of 2.56 mA is not enough for MCUs in eIoTs and its 650 nA quiescent current also limits the further reduction of the power consumption.

To solve the above issue, the paper proposes several techniques for power management in the low-power MCU for eIoT with low cost and high reliability. Firstly, the application-based multimode switch scheme along with a multipower domain strategy is proposed to optimize the power consumption through a hierarchical control. In addition, we integrate the traditional power switch function into the chip, effectively reducing the system cost and extending the battery life. In order to further reduce the power consumption in the sleep mode, we design an ultra-low-power backup power supply circuit in lieu of the traditional LDO in the sleep mode, reducing the power to 0.1 μA.

The paper is organized as follows. Section 2 introduces the architecture of the power management system in the

MCU for the eIoT. Section 3 describes the proposed ultra-low-power backup LDO circuit design, followed by measurement results in Section 4. Section 5 concludes the work.

2. Design of Low-Power Supply System with High Reliability

In order to effectively simplify the peripheral circuit design and prolong the battery life, the independent power supply mechanism of the RTC and the corresponding main power supply, battery power supply, RTC power supply, and other multipower domain switching strategies and multiple low-power operation modes are designed.

2.1. Application-Based Multimode Switching Scheme. In view of the complexity characteristics of the of eIoT applications, five working modes are designed according to the different applications of the MCU, namely, active, idle, sleep, deep sleep, and RTC-only, to reduce the power consumption of the chip. Take the energy meter as an example [14]: the active mode is applied when the meter is running normally; the sleep mode is used in scenarios where the meter is powered by battery supplies during a power outage; the deep sleep mode can further reduce power consumption of the sleep mode shutting down more functions; and the RTC-only mode is suitable for extremely low power running when the meter is placed in the warehouse and not yet mounted [15]. The switching of these five working modes is shown in Figure 1.

The idle and sleep modes are directly controlled by the MCU core, and users only need to execute specific instructions to enter in or out of these modes. The control of the
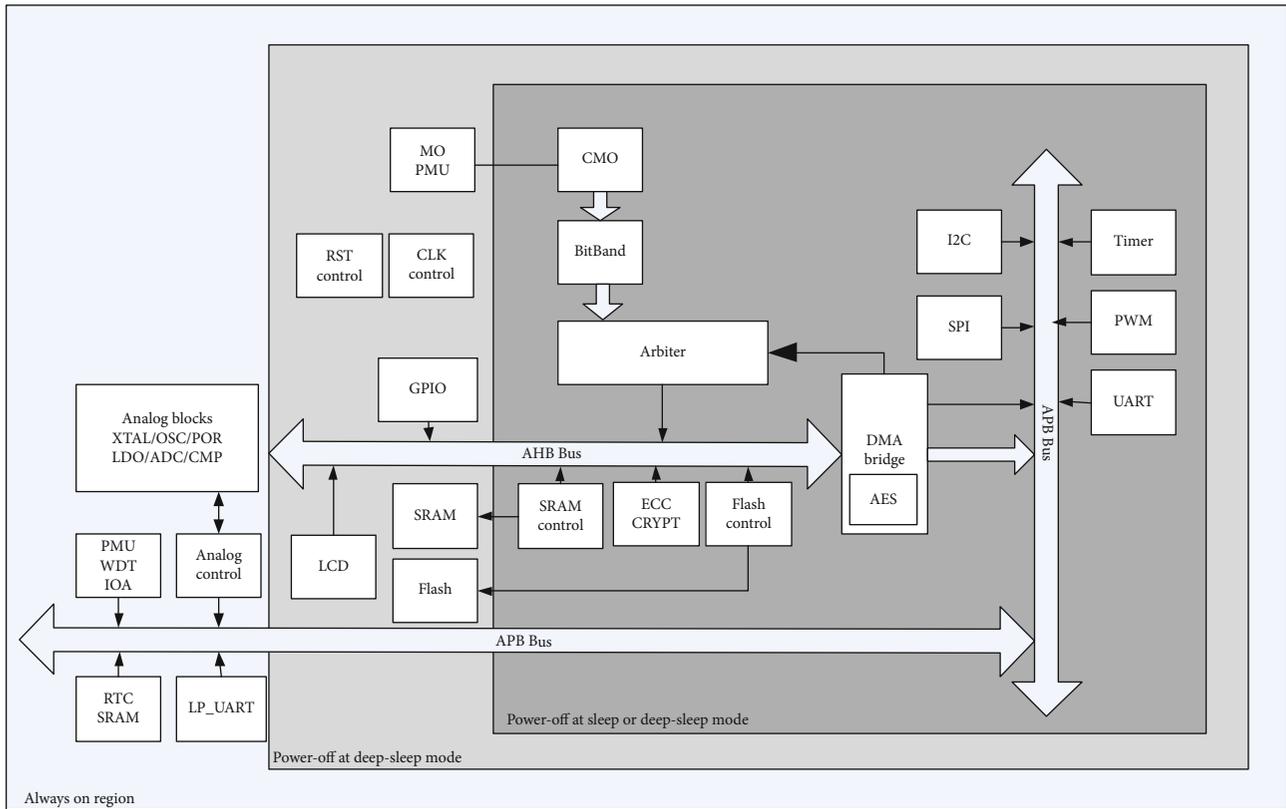
FIGURE 2: System functional block diagram.

deep sleep and RTC-only modes is realized through the power management unit (PMU). By reading the value of the control register written by the software, the PMU controls the hardware state machine to switch between different modes. The involved operations include the power gating and clock gating of the corresponding modules [16, 17] and the isolation of different power domains. To explain different modes, we show the system functional block diagram in Figure 2 with power domains. The specific working status of different modes is as follows:

(1) Active

This mode is the normal working mode of the MCU. In this mode, the chip works at the PLL clock or internal high-frequency RC clock, the CPU core is turned on, and the functional modules, interfaces, and peripherals can all be turned on and configured through the software.

(2) Idle

In this mode, the CPU is stopped, but the high-speed peripherals remain monitoring and can be quickly awakened by any interruption.

(3) Sleep

In this mode, the CPU and most functional modules are turned off. Only SRAM, PMU, GPIO, etc. are working. As shown in Figure 2, the dark gray part is powered off. The

TABLE 1: Power supply in different modes of the chip.

| MODE | Main power domain | | RTC domain |
	VDD	BATVDD	BATRTC
Active	V		
Idle	V		
Sleep		V	
Deep sleep		V	
RTC-only			V

high-frequency clock is turned off. The chip works using the low-frequency clock RTCCLK.

(4) Deep sleep

In this mode, the CPU and all peripherals are powered down, and only the interrupting IOs, RTC, PMU, and UART32K (low-power UART module) modules are active. As shown in Figure 2, the light gray part is also powered off.

(5) RTC-only

All main power supplies are powered down, and only the RTC circuit powered by BATRTC maintains operation in this mode, as shown in the blue part in Figure 2.

For energy meters, the power supplies in different modes are also different, as shown in Table 1. In normal mode, the chip uses the main power supply VDD. It is usually supplied by a rectifier bridge and an LDO. In this power supply
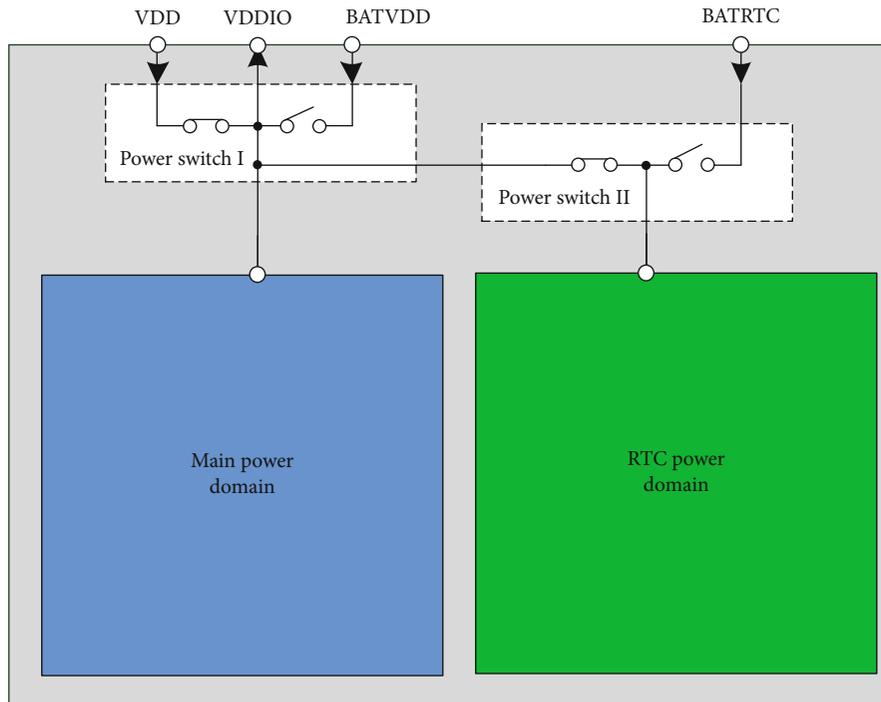
FIGURE 3: Independent power supplies for multiple power domains.

situation, the chip can also enter the idle mode to save energy. When the main power is off, such as in the case of storage or power outage, the battery will be activated as a backup power source to maintain the basic function of the chip. The chip then transitions into the sleep or deep sleep mode. The RTC must be accurate under all conditions. Therefore, a special RTC power domain is designed. It is powered by another separate battery and kept always on. When the main power domain is completely powered off, the chip enters the RTC-only mode.

2.2. Built-In Power Switching with High Reliability. As shown in Figure 3, the power architecture of the chip is divided into two parts. One is the main power domain, under which most functional modules such as the CPU, memory, and peripherals are placed. The other is the RTC power domain. This domain has the always-on circuits such as the crystal oscillator clock and RTC module. Except for in the RTC-only mode, the main power domain is always on. When the utility power is present, it is powered by the utility power, and during a power outage, it switches to the battery power. Usually, this switching is done off-chip. As shown in Figure 4(a), in order to prevent the reverse current, the regulated main power and the battery are, respectively, connected in series with a diode and then supplied to the chip's supply input VDD. Generally, the voltage of the regulated utility power is higher than that of the battery, so the chip is powered by the utility power. In addition to the BOM cost of the diode, this scheme also has a disadvantage of the diode voltage drop. The diode voltage drop can reduce the battery usage range.

To solve this issue, this work proposed a built-in power switching with high reliability. In this design, the main power domain is changed from the traditional single-power input (VDD in Figure 4(a)) structure to a three-power structure, including the main power input VDD, battery input BATVDD, and IO power (the main power supply of the chip generated after the power selection). When implemented, as shown in Figure 4(b), VDD and BATVDD are connected to VDDIO through a MOSFET switch, respectively, and the control logic ensures that only one switch is turned on at a given time. VDDIO is connected to VDD by default. VDD is divided by a series of resistors and then connected to the hysteresis comparator for the voltage detection. When VDD is lower than the switch threshold, VDDIO is switched to the battery. To address potential reliability issues during usage, the switching circuit is designed carefully as follows.

In most cases, the VDDIO voltage is close to the higher of these two inputs. Considering that the voltage of VDD may be 3.3 V or 5.0 V, while that of BATVDD is usually 3.6 V (at full capacity), the bulk of the two switch MOSFETs is connected to VDDIO to ensure that the source and drain of the MOSFETs are reverse biased to the bulk parasitic diode. BATVDD, as a backup power supply, does not provide current to circuit to prolong the life of the battery unless the main power is off. Therefore, the power supply switching is only controlled by detecting VDD. Generally, the switching threshold for 5 V (main supply voltage) applications is 3.6 V, and for 3.3 V application is 3.0 V.

As shown in Figure 5, the output of the detection circuit is connected to the power switch circuit to generate two-phase nonoverlapping clocks [18, 19]. One of the clock signals passes through a buffer and is used to control the switch of VDD. Because PM0 is usually kept on during the normal application, the driving capacity of PM0 should be large
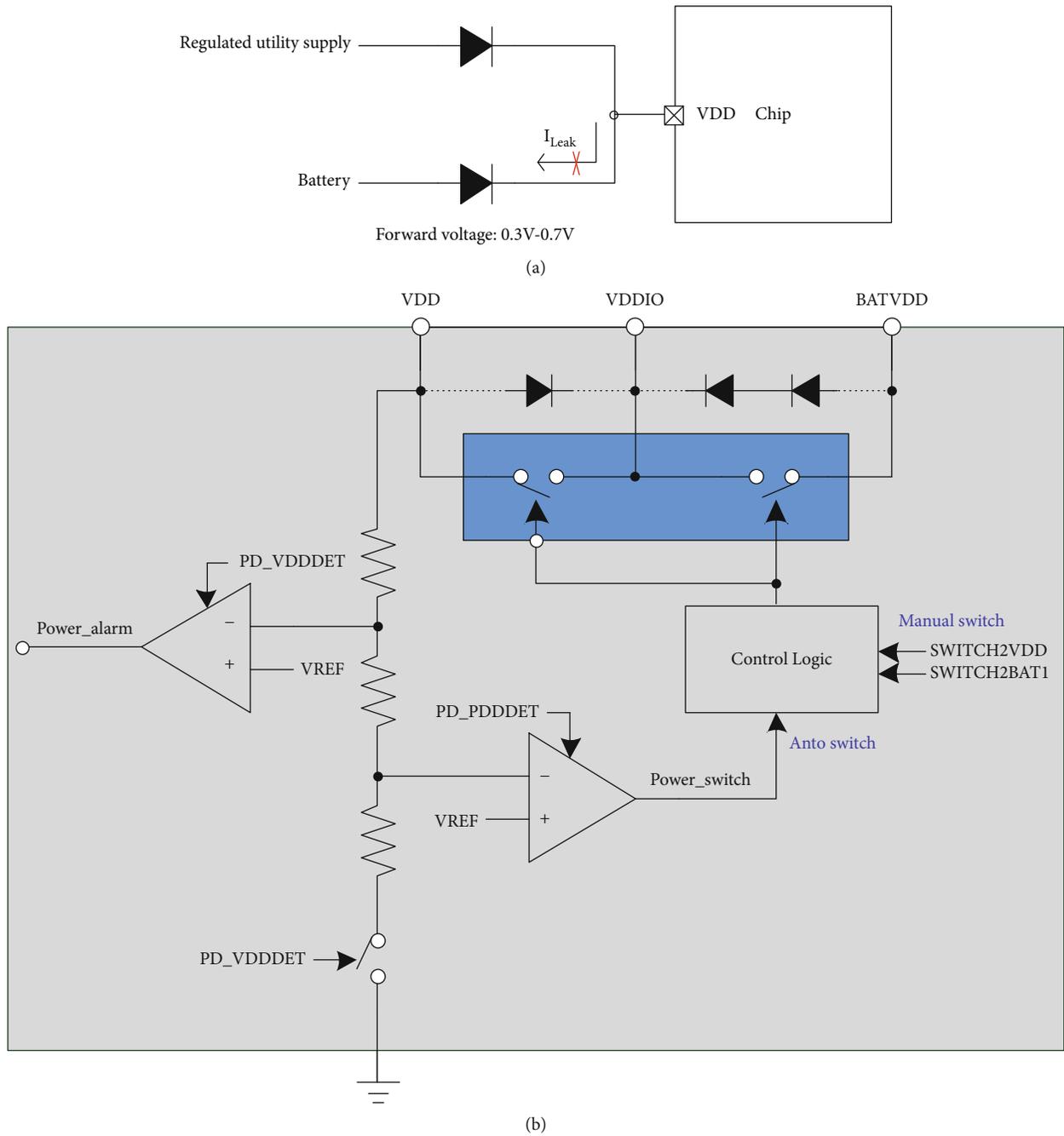
FIGURE 4: (a) Traditional external switching scheme; (b) proposed internal switching scheme.

enough. In order to reduce the area, a low-voltage PMOS with a larger current density per unit area is used. But meanwhile, it is necessary to control the gate-source voltage V_{GS} of PM0 to avoid breakdown. In this design, a voltage drop close to 1.5 V is generated through two diode-connected MOS transistors through a fixed bias current. When PM0 is turned on, PM7 and PM8 produce a voltage drop. When PM0 needs to be turned off, PM9 connects the gate of PM0 directly to the source. The other clock signal is used to generate the switch control signal of PM1. In order to ensure that PM1 can be completely shut down, it is necessary to ensure that the gate

voltage of PM1 follows the source voltage (the source is of a higher voltage than the drain). Therefore, the gate voltage of PM1 needs to be at the higher voltage of VDDIO and BATVDD to prevent the reverse current to the battery when VDDIO = VDD = 5 V. The detailed circuit is shown in Figure 5. When PM0 is turned on, S2 is low. PM3 and PM4 are on, and NM0 and NM1 are off. PM5 and PM6 are gate-source connected transistors that act like parasitic diodes. Since there is no conduction current, the voltage drop is much smaller than a threshold voltage V_{TH}, so that the voltage of the gate of PM1 is almost equal to the higher voltage of
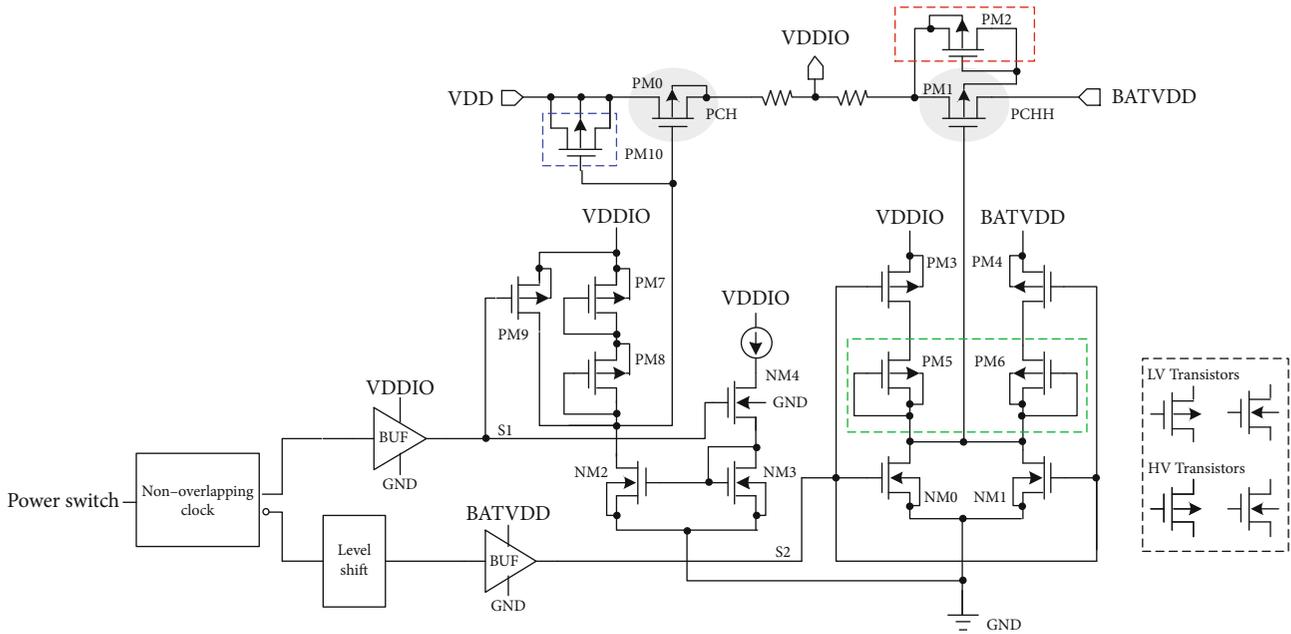
FIGURE 5: Power supply switching circuit.

M0(2.96, −622.8 uA)

—— The bulk of PM2 is directly connected to the source
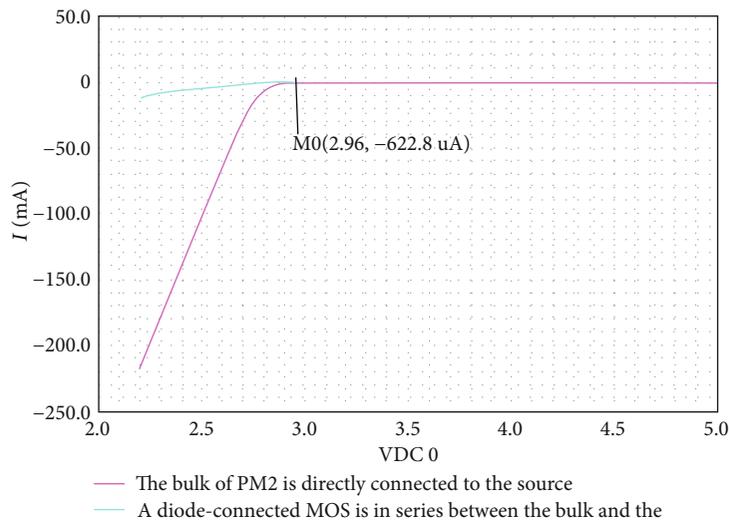—— A diode-connected MOS is in series between the bulk and the

FIGURE 6: BAT leakage current with and without PM2.

VDDIO and BATVDD. With PM5 and PM6, the two power supplies can also be isolated from each other to prevent the inverse current.

An additional transistor PM2 is connected on the bulk of PM1 to avoid drawing current from the battery. For 3.3 V applications, the threshold of the power switch is set at 3.0 V ± 10%. It may happen that PM1 remains off, but the parasitic diode of its drain and bulk is forward biased and starts to draw current from BATVDD without PM2 [20]. The effect is similar to doubling the threshold voltage from BATVDD to VDDIO, as shown in Figure 4(b), which improves the reliability of the power supply switching circuit. The comparison is shown in Figure 6. When VDDIO is lower than 3.0 V, BATVDD starts to leak current to VDDIO, and the modified circuit has significantly smaller leakage than the original circuit.

The transistor PM10 is also connected in series at the drain and gate of PM0 to solve the breakdown problem that may be caused by the rapid rise of VDD with the cold start. Through the MOS CAP formed by PM10, the instantaneous voltage difference between the drain and the gate of PM0 is limited. It also improves the reliability of the circuit [21].

To ensure that bulk parasitic diodes of these two power switches PM0 and PM1 are always reverse biased, the conduction voltage drop of both should be small enough. Under the condition that the maximum load current is 30 mA, the selected conduction impedance is less than 8 Ω over process corners.
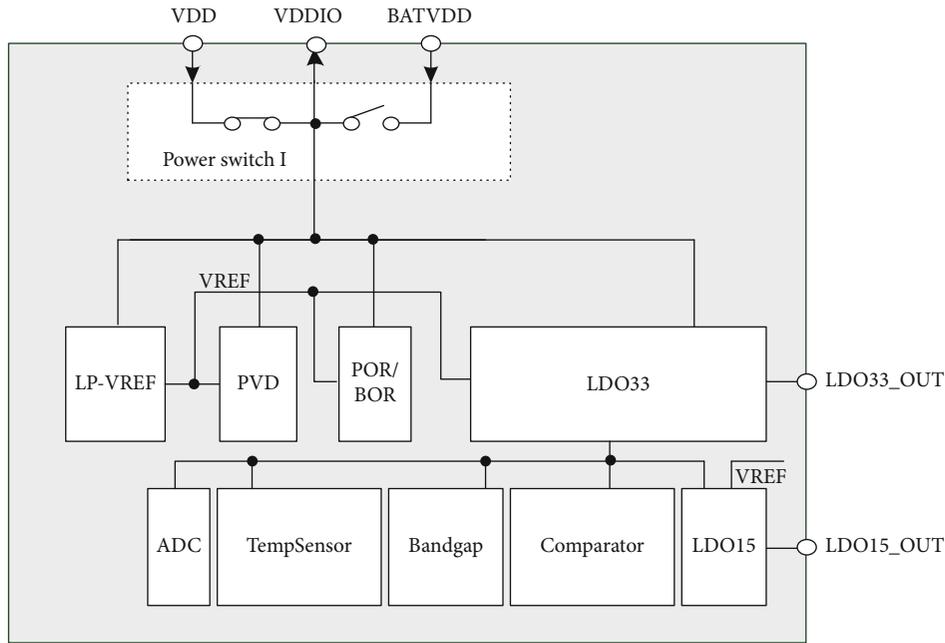
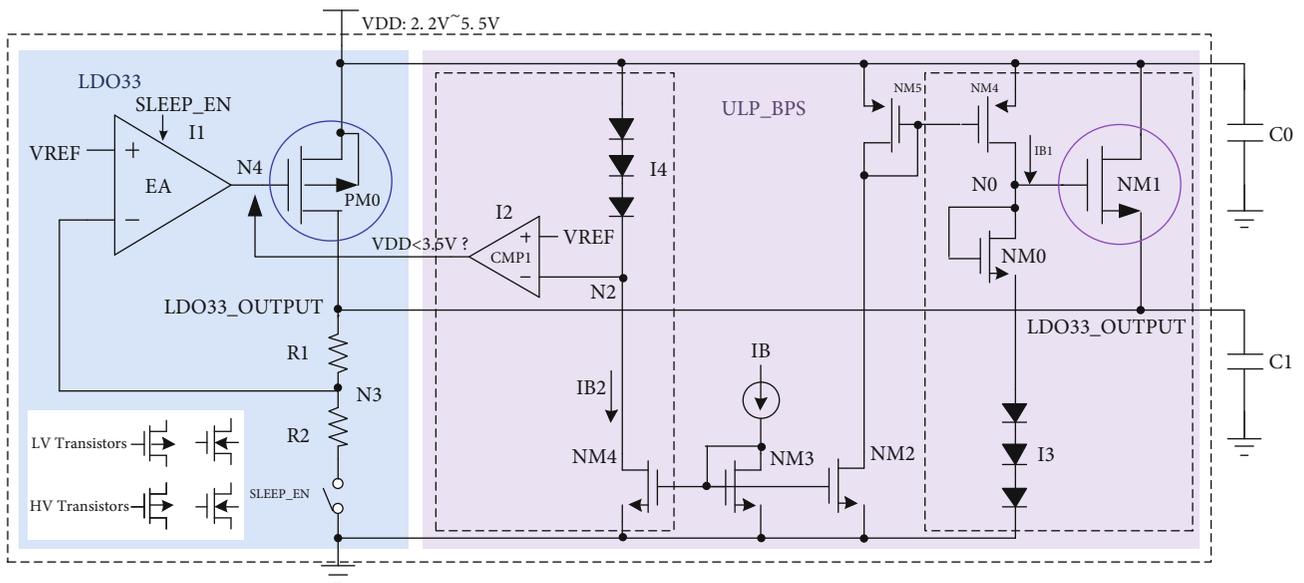Figure 7: BAT leakage current with and without PM2.

Figure 8: Ultra-low-power backup power supply (ULP_BPS).

As for the power switch in the RTC power domain (power switch I in Figure 3), because the RTC power domain continues to work at low power consumption (such as 1 μA), the design of the switch is similar, but it will be much simpler.

3. Ultra-Low-Power Backup Power Supply Design

MCUs usually have multiple power supplies from different sources, such as from an off-chip LDO output, by an ultracapacitor, or from a battery, depending on the applications. To ensure that the key modules have a stable power supply voltage, as shown in Figure 7, MCUs with a 5 V main supply volt-

age usually regulate the supply voltage to 3.3 V through an internal LDO (referred to as LDO33 below) to supply analog modules such as the bandgap, the temperature sensor, and ADC. It is also used to supply current for low-power-consuming blocks such as the LDO15 and comparators. In the sleep mode with the main power on, the LDO33 is still active because some of the analog blocks are still working. To achieve lower power consumption in the sleep mode, the quiescent current of the LDO33 needs to be minimized.

The traditional LDO33 is shown in Figure 8. The output voltage is divided by the sampling resistor and fed back to the error amplifier (EA) to generate a stable voltage LDO33_OUT. To design a low-power LDO, in addition to reducing
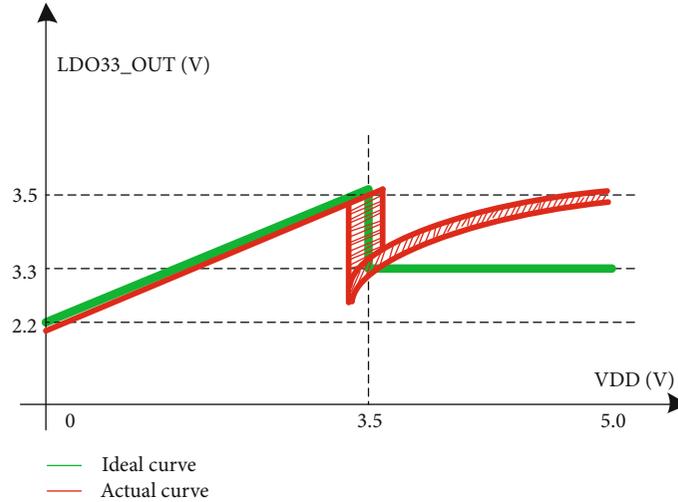
FIGURE 9: Ideal output vs. output considering nonideal effects.

the power consumption of the EA block, it is also necessary to minimize the current on the sampling resistors. Because the voltage drop of the resistor is fixed, the current can only be reduced by increasing the resistance. A larger resistance leads to a larger area. Suppose we want to reduce the power consumption of the LDO33 to $0.1\,\mu$A, using the traditional scheme, the resistance needs to be increased to $33\,$M ohms even without considering the power consumption of the EA. A $33\,$M ohm resistance in a CMOS process is usually area consuming. As for the digital LDO, it can work at a very low supply voltage, but it usually has the problem of large output ripple and it is still challenging to achieve absolute low power consumption [22], which is not suitable for the target applications.

In the sleep mode, the most functional modules are turned off; the load of LDO33 usually does not exceed $100\,\mu$A. The accuracy of the output voltage is also greatly relaxed. The paper proposes to add an ultra-low-power backup power supply (ULP_BPS) to the traditional LDO33. In the sleep mode, the main LDO is shut down and the ULP_BPS kicks in to reduce the power consumption.

As shown in Figure 8, LDO33_OUTPUT (the output voltage) is generated by passing a fixed voltage through a source follower. The required voltage is generated by adding a bias current to the diode string. The bias current can be limited to $10\,$nA and provided by anther low-power reference and bias generation circuit, which consumes about $300\,$nA and can also provide the reference voltage VREF for LDO33 in the normal working mode. It is powered by the main supply voltage VDD to avoid start-up problems. Due to the use of the source follower structure, there is no need for a resistor string to form a feedback loop and no need to worry about the stability.

In this implementation, the P-type bias current flows thru a diode-connected transistor NM0 and a diode string I3 to the ground. If the gate-source voltage V_{GS} of NM0 is close to that of the driver transistor NM1, the output LDO33_OUT (the source of NM1) is almost equal to the

voltage across I3. Therefore, the output voltage can be adjusted by adjusting the number of diodes in I3. When VDD is small (less than $V_{I3} + V_{GS,NM0}$), the transistor NM4 enters the linear region, and the output voltage is about $V_{DD} - V_{GS,NM1}$.

Since the battery voltage changes in its lifetime, the MCU is usually required to have a wide operating voltage range, such as $2.2\,$V~$5.5\,$V. But the analog blocks supplied by LDO33 have a minimum voltage requirement, say $2.2\,$V. When the voltage is lower than this, the analog blocks will work abnormally, and the chip will also trigger power on reset (POR) and exit the sleep mode. In this case, LDO33 will follow VDD directly, regardless of the level of VREF. VREF is calibrated to guarantee the accuracy of the supply detection result. In summary, ULP_BPS block needs to meet the requirements of $2.2\,$V~$3.8\,$V output under $2.2\,$V~$5.5\,$V input. The $3.8\,$V output is due to the requirement of the device breakdown voltage.

When the input is low, say below $3.0\,$V, the output $V_{DD} - V_{GS,NM1}$ will be difficult to maintain above $2.2\,$V. We add a power detection mechanism to address this. When a low-power supply voltage is detected, the driver transistor PM0 is turned on such that the output of LDO33_OUT follows VDD to maximize power utilization. The driver transistor of the main LDO can be reused to ensure a low voltage drop while avoiding additional area cost. In the implementation, a fixed bias current flows through the diode string I4 connected to VDD to generate a voltage drop $V_{DD} - V_{I4}$ that is compared with the low-power reference voltage VREF through a comparator. For example, if the voltage drop across I4 is designed to be $2.3\,$V, the output will follow VDD when VDD is lower than $3.5\,$V (VREF is about $1.2\,$V).

In CMOS processes, diodes are generally realized by diode-connected MOS transistors. In order to ensure that the output is controlled within the demand range for different loads, power supply sources, temperatures, and process deviations, it is necessary to minimize the variation of the device to achieve bias in the design with respect to the above
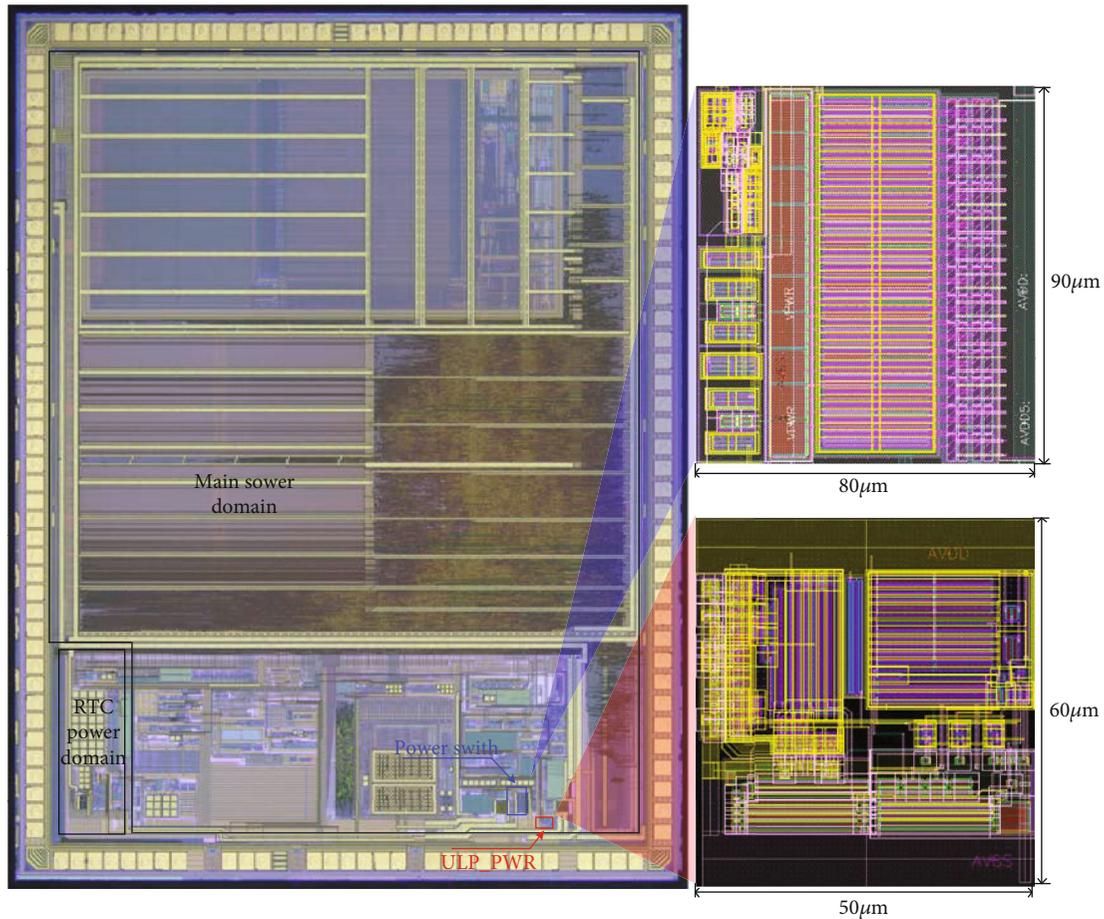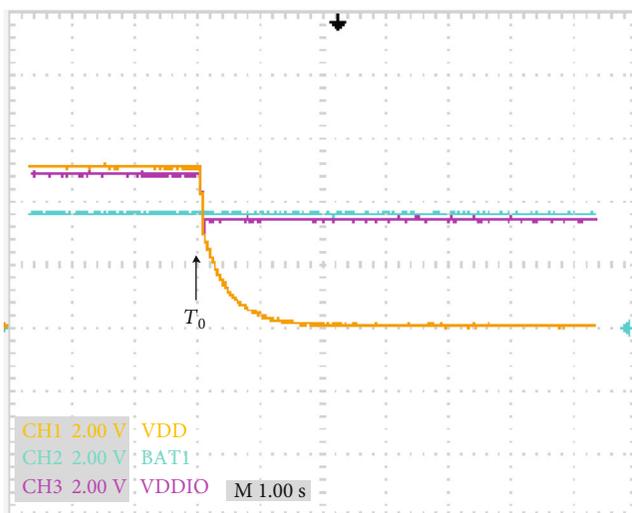
Figure 10: Die microphoto.

Figure 11: Oscilloscope results of power switch scheme.

variables [23]. Figure 9 shows the simulated output voltage vs. the VDD. Detailed design considerations for high reliability are list below.

The typical voltage drop at I4 is $V_{DD} - V_{REF} = 2.3$ V, lower than the breakdown voltage of the low-voltage transistor. It is realized by using three low-voltage (LV) PMOS in series. For the diode string I3, a high-voltage (HV) IO PMOS is used to avoid breakdown of LV devices. However, the threshold voltage of HV PMOS is relatively high, and it cannot match 3.3 V well if two or three are connected in series, so a small LV core NMOS is used at the end of series closest to GND. A MOS transistor of the same type as NM1 is used to implement NM0 so that the gate-source voltage VGS is as close as possible. However, due to the difference in current flow, variations will still be introduced. The body of the HV PMOS is connected to VDD. When the input is over 3.6 V, the actual output is a curve that increases with VDD but the slope gradually decreases as shown in Figure 9. The output is shown in the red curve in Figure 9. The turning point and the output at high VDD have a certain offset range, but it does not exceed the target window of 2.2 V-3.5 V.

In the design, the bulks of all PMOS transistors are not connected to the source to eliminate the body effect. The main consideration is that the branch bias current is very small so the impedance is high. During reliability tests such as latch-up, if there is substrate leakage, it may cause abnormal bias, so the bodies of transistors are connected to a low-resistance power supply or ground.

TABLE 2: Comparison of results between traditional LDOs and the improved structure.

Module	Technology (μm)	Input voltage (V)	Output voltage (V)	Max output current (mA)	Quiescent current (μA)	Size (mm^2)	Stability consideration
LDO33 (this work)	0.11	2.2-5.5	2.2-3.6	30	1	0.026	Yes
ULP_BPS (this work)	0.11	2.2-5.5	2.2-3.8	0.1	0.1	0.003	No
Adaptive LDO [13]	0.13	1.9-3.6	1.52	2.56	0.65-17.7	0.016	Yes
DLDO [22]	0.65	0.5	0.45	0.2	2.7	0.042	Yes
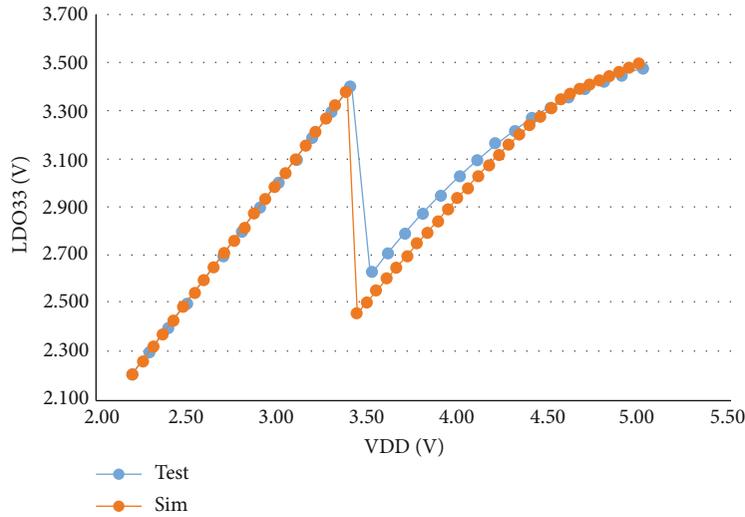
(a)
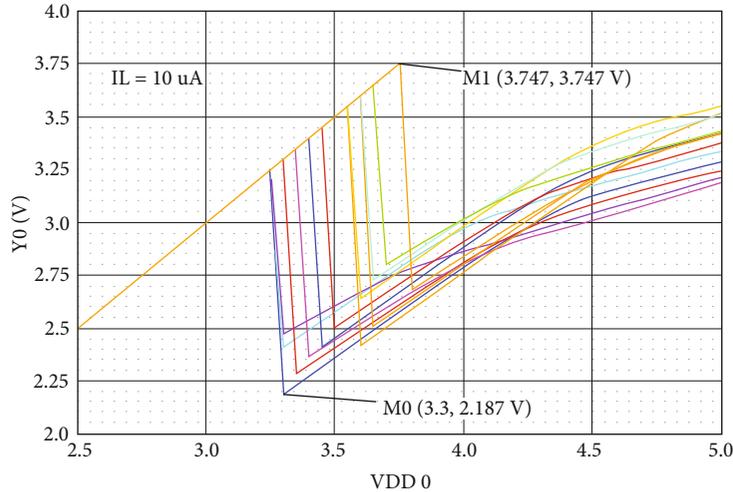
(b)

FIGURE 12: (a) Simulation result vs. test result; (b) impact of PVT on turning point.

4. Simulation and Test Results

The design is implemented in a standard 0.11 μm CMOS process. As shown in Figure 10, the area of the power supply switching circuit and the low-power backup power supply is 0.0072 mm^2 and 0.003 mm^2, respectively, accounting for less than 1% of the whole chip area.

To test the power switching circuit for an actual energy application, we connect BATVDD to 3.6 V and VDD to 5.0 V DC sources, respectively. Enable the automatic
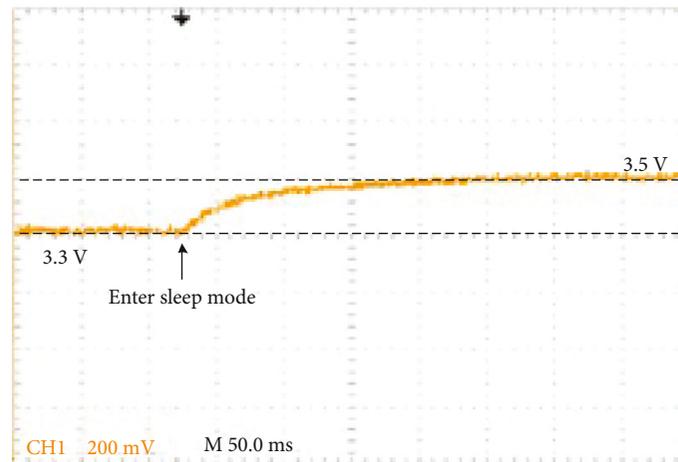
FIGURE 13: Measurement results of LDO33_OUT using an oscilloscope when switching from the normal operating mode to the sleep mode.

switching mode, and set the switching voltage to 3.6 V through software configuration, then disconnect VDD from the DC source at T_0, and observe the entire switching process through an oscilloscope. In Figure 11, the yellow line and the blue line are the two input power supplies, VDD and BATVDD, respectively, and the purple line is the output VDDIO. It can be seen that after disconnecting from the DC source, VDD drops slowly, and VDDIO still follows VDD at the beginning. But when it drops to about 3.6 V, VDD continues to drop, and VDDIO remains near the battery voltage. The realization of the entire power switch is stable and reliable.

Test results show that the power consumption of the proposed ULP_BPS module is about 0.1 μA, which is an order of magnitude lower than the power consumption of the traditional low-power LDO33. Due to the open loop structure, it does not have stability problem. Compared to single adaptive LDO design in [13], this work can achieve lower quiescent current and support larger load current (30 mA) by combining the traditional LDO33 and the proposed ULP_BPS. Comparison of results is shown in Table 2.

Set the output current of LDO33_OUT to 5 μA, and perform a DC swept on VDD from 5 V to 2.2 V. Both the simulation and test results are shown in Figure 12(a), meeting the design spec. Figure 12(b) shows the influence of Process-Voltage-Temperature (PVT) on the output. It can be seen that the output is 2.2 V~3.75 V under the full input range of 2.2 V~5.5 V meeting the design spec.

In practical applications, when the energy meter enters the sleep mode from the normal operating mode, the output of LDO33_OUT is observed through the oscilloscope, as shown in Figure 13. Because LDO33 has a large decoupling capacitor off-chip, e.g., 10 μF, LDO33_OUT will slowly switch to the output of ULP_BPS.

5. Conclusions

To address the low-power design issue for MCU, we proposed several power management techniques. Firstly, the application-based multimode switch scheme along with a multipower domain strategy is proposed to optimize power consumption through hierarchical control. In addition, we integrated the traditional power switching function into the chip and designed a safe and reliable power switch circuit, which can effectively reduce system costs and extend battery life. To further reduce the power consumption in the sleep mode, we also designed an ultra-low-power backup power supply circuit to replace the low-power LDO reducing the power to 0.1 μA, an order of magnitude lower than the original circuit. The techniques have been used in energy metering chips that have been sold in millions.

Data Availability

The data used to support the findings of this study are included within the article.

Conflicts of Interest

There is no conflict of interest regarding the publication of this paper.

References

[1] T. K. Chien, L. Y. Chiou, S. S. Sheu et al., "Low-power MCU with embedded ReRAM buffers as sensor hub for IoT applications," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 6, no. 2, pp. 247–257, 2016.

[2] B. A. Khan and H. M. Ashraf, "Implementation of micro controller based electromechanical over current relay for radial feeder protection," in *2019 international conference on engineering and emerging technologies (ICEET)*, Nagoya, Japanese, 2019.

[3] D. Abbasinezhad-Mood and M. Nikooghadam, "An ultra-lightweight and secure scheme for communications of smart meters and neighborhood gateways by utilization of an ARM Cortex-M microcontroller," *IEEE Transactions on Smart Grid*, vol. 9, no. 6, pp. 6194–6205, 2018.

[4] X. Fang, S. Misra, G. Xue, and D. Yang, "Smart Grid - the new and improved power grid: a survey," *IEEE communications surveys & tutorials*, vol. 14, no. 4, pp. 944–980, 2012.

[5] S. M. Bashi, N. Mariun, and A. Rafa, "Power transformer protection using microcontroller-based relay," *Journal of Applied Sciences*, vol. 7, no. 12, pp. 1602–1607, 2007.

[6] F. R. Clenitiaa, E. Ilakya, G. S. Preetha, and B. Meenakshi, "Enhanced digital energy meter," in *2017 International Conference on Computation of Power, Energy Information and Commuincation (ICCPEIC)*, pp. 588–591, Melmaruvathur, 2017.

[7] M. Natsui, Y. Noguchi, M. Yasuhira et al., "A 47.14- μW 200-MHz MOSMTJ-hybrid nonvolatile microcontroller unit embedding STT-MRAM and FPGA for IoT applications," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 11, pp. 2991–3004, 2019.

[8] A. I. Lita, D. A. Visan, M. Gherghe, L. M. Ionescu, A. G. Mazare, and I. Lita, "Microcontroller based magnetometer for smart meters used in electrical energy measurement," in *2018 41st International Spring Seminar on Electronics Technology (ISSE)*, pp. 1–4, Zlatibor, 2018.

[9] H. Jian and S. Xubang, "The design methodology and practice of low power SoC," in *2008 International Conference on Embedded Software and Systems Symposia*, pp. 185–190, Sichuan, 2008.

[10] Z. Jing-Jing and L. Feng, "System-level power management for low-power SOC design," in *2011 10th international symposium on distributed computing and applications to business, Engineering and Science*, pp. 412–416, Wuxi, 2011.

[11] X. Zhang, H. Jiang, B. Zhu, X. Chen, C. Zhang, and Z. Wang, "A low-power remotely-programmable MCU for implantable medical devices," in *2010 IEEE Asia Pacific Conference on Circuits and Systems*, pp. 28–31, Kuala Lumpur, 2010.

[12] Datasheet of STM32L010RB [M], DS12319 Rev 3, and STMicroelectronics, "Ultra-low-power value line Arm Cortex-M0+ MCU with 128-Kbytes of Flash memory, 32 MHz CPU [DB/OL]," 2019, https://www.st.com/resource/en/datasheet/stm32l010rb.pdf.

[13] M. Lueders, B. Eversmann, J. Gerber et al., "Architectural and circuit design techniques for power management of ultra-low-power MCU systems," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 22, no. 11, pp. 2287–2296, 2014.

[14] Z. Zhimei, Z. Dongyan, and Z. Haifeng, "Research on the key technology of the dual MCUs on the energy meter for the IR46 standard," *Application of Electronic Technique*, vol. 10, 2017.

[15] Z. Dong-yan, Z. Zhi-mei, Y.-b. Wang, and Z. Haifeng, "A RTC compensation arithmetic and circuit based on cumulated deviation limitation," *Application of Electronic Technique*, vol. 40, no. 12, 2014.

[16] R. N. Agnes Shiny, B. Fahimunnisha, S. Akilandeswari, and S. J. Venula, "Integration of clock gating and power gating in digital circuits," in *2019 5th international conference on Advanced Computing & Communication Systems (ICACCS)*, pp. 704–707, Coimbatore, India, 2019.

[17] N. Anand, G. Joseph, and S. S. Oommen, "Performance analysis and implementation of clock gating techniques for low power applications," in *2014 International Conference on Science Engineering and Management Research (ICSEMR)*, pp. 1–4, Chennai, 2014.

[18] R. Spilka, G. Hilber, A. Rauchenecker, D. Gruber, M. Sams, and T. Ostermann, "Generation of non-overlapping clock signals without using a feedback loop," in *2012 IEEE 15th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS)*, pp. 219–223, Tallinn, 2012.

[19] B. Nowacki, N. Paulino, and J. Goes, "A simple 1 GHz non-overlapping two-phase clock generators for SC circuits," in *Proceedings of the 20th International Conference Mixed Design of Integrated Circuits and Systems - MIXDES 2013*, pp. 174–178, Gdynia, 2013.

[20] S. M. Sze, *Physics of Semiconductor Devices*, Wiley, New York, 1981.

[21] P. E. Allen and D. R. Holberg, *Cmos Analog Circuit Design 2E*, Publishing House of Electronics Industry, 2007.

[22] Y. Okuma, K. Ishida, Y. Ryu et al., "0.5-V input digital LDO with 98.7% current efficiency and 2.7-μA quiescent current in 65nm CMOS," in *IEEE Custom Integrated Circuits Conference 2010*, pp. 1–4, San Jose, CA, 2010.

[23] S. Chandra, K. Lahiri, A. Raghunathan, and S. Dey, "Variation-tolerant dynamic power management at the system-level," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 17, no. 9, pp. 1220–1232, 2009.