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Research Article

A Glitch-Free Novel DET-FF in 22 nm CMOS for Low-Power Application

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Dual edge triggered (DET) techniques are most liked choice for the researchers in the field of digital VLSI design because of its high-performance and low-power consumption standard. Dual edge triggered techniques give the similar throughput at half of the clock frequency as compared to the single edge triggered (SET) techniques. Dual edge triggered techniques can reduce the 50% power consumption and increase the total system power savings. The low-power glitch-free novel dual edge triggered flip-flop (DET-FF) design is proposed in this paper. Still now, existing DET-FF designs are constructed by using either C-element circuit or 1P-2N structure or 2P-1N structure, but the proposed novel design is designed by using the combination of C-element circuit and 2P-1N structure. In this design, if any glitch affects one of the structures, then it is nullified by the other structure. To control the input loading, the two circuits are merged to share the transistors connected to the input. In the proposed design, we have used an internal dual feedback structure. The proposed design reduces the delay and power consumption and increases the speed and efficiency of the system.

1. Introduction

Today, the flip-flops are widely used for data storage. The performance and fault tolerance ability of the devices are precisely affected by the flip-flops reliability, speed, and power consumption. As a result, this is needed to design the flip-flops for lowest power consumption, propagation delay, area, and highest reliability with fault tolerance ability. Present studies have shown that device scaling reduces the device capacitances and the supply voltage requirements, and circuit becomes more vulnerable to the glitches. When particles touch the drain side of a MOSFET, electron hole combinations are generated. The reverse biased electric field produces a drift transient current [1, 2]. Voltage transient as a result of the collected charge is called a transient fault. In memory elements, transient faults may be produced by the preceding combinational circuit glitches.

Low-power consumption may be obtained efficiently by voltage supply scaling. In CMOS designs, power consumption due to the glitches cannot be ignored as the portion of power consumption varies somewhat between 9% and 38% [3]. Today, in digital integrated circuits, the designing of energy efficient designs is one of the great challenges for the researchers [4]. Power consumption in clock distribution network is very significant, which may account 45% of the total system power [5]. Clock network consumes more power; consequently, this is necessary to reduce the number of overall clocks. To reduce the number of clocks, the true single-phase clock (TSPC) technique has been advised with the basic registers [6]. To reduce the clock power consumption, the clock frequency can be scaled down, by sampling the data on both of the falling and rising edges of the clock, without altering the system throughput. The dual edge triggered procedure reduces the 50% power dissipation of the clock network system. However, dual edge triggered designs are more complex as compared to single edge triggered (SET) designs, but this can be more energy efficient [7].

The rest part of this paper is arranged as follows. Section 2 reports the existing designs. We have interpreted the proposed work in Section 3. Section 4 describes the result and analysis. Finally, Section 5 concludes this work.

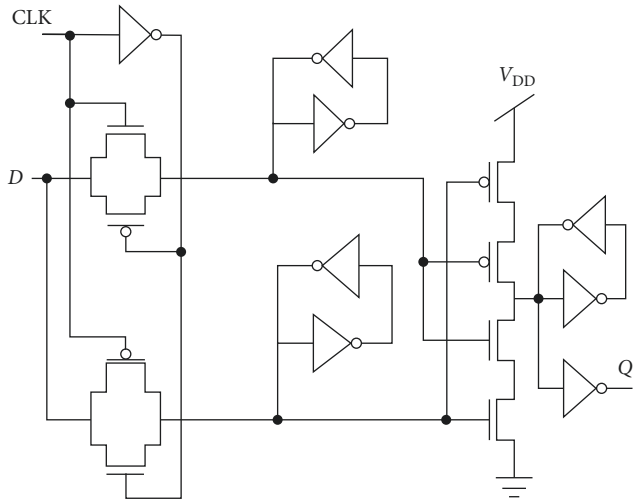

Figure 1: DDR-FF (LM_C) design [10].

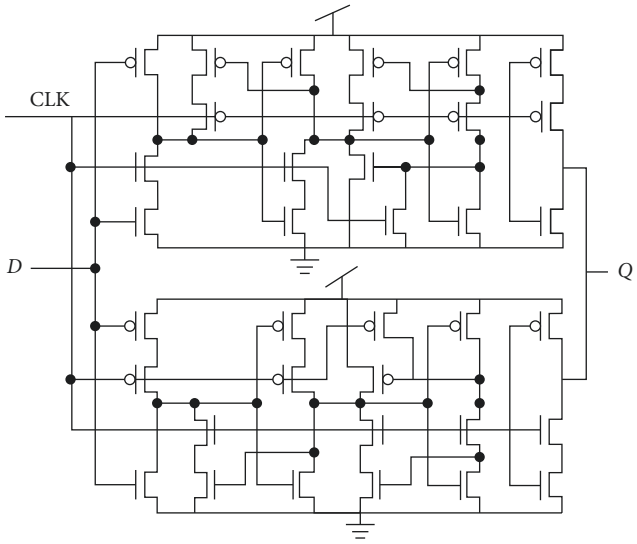

Figure 2: TSPC design [11].

2. Existing Designs

Dual edge triggered flip-flops provide the equal data rate as single edge triggered flip-flops at the half of the clock frequency, which leads to the reduction in power dissipation of digital synchronous logic designs [8, 9]. Figure 1 shows the dual data rate flip-flop (DDR-FF) which has a lower clock load because of its simple configuration, lower activity factor, and hard edge quality factor [10]. Devarapalli et al. [10] presented a robust LM_C dual edge flip-flop by using C-elements, where the direct clock pulses were used to latch the data for the reduction of clock dynamic power consumption without any additional pulse generator circuit. This flip-flop design offers the more robust solution for dual data rate (DDR) flip-flops due to its simplicity with less number of transistors. Bonetti et al. [11] proposed a dual edge triggered flip-flop, as shown in Figure 2, to overcome the built-in clock overlap threat, by using true single-phase clock circuits instead of an inverted clock and clarify the issue of clock overlapping by using the TSPC circuits and an internal dual feedback structure.

Figure 3 shows the LG_C circuit design [12] which improved with common Latch MUX dual edge triggered flip-flops; because of this fact, flip-flops internal circuit node value never changes with the changes in the input value. The LG_C circuit design presented improvement in the energy dissipation. The glitch-free LG_C dual edge triggered flip-flop was designed by three C-element circuits, with two internal latches A and B and one output latch Q, with inverting topology because of the transistor level implementations.

Generally, the C-element structures are used to reduce the switching activity. The 2P-1N three-transistor structure [13] and C-element circuit [14] and their truth tables are shown in Figure 4. The C-element structure is a 3-terminal structure with the two inputs and a single output. The C-element circuit has the special feature that when both inputs are equal, thereupon output switches to its input values; when the inputs are not equal, thereupon its output goes to the high impedance state, which means output will be in its past state. The 2P-1N three-transistor structure is

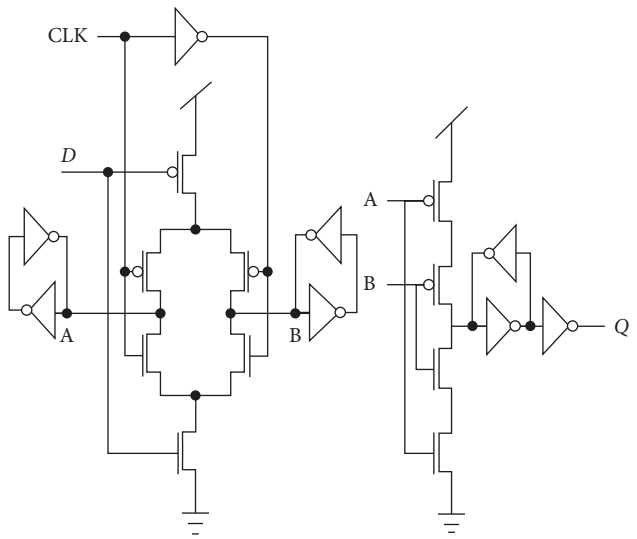

Figure 3: LG_C design [12].

different from the C-element circuit: (1) when the inputs are not equal, then the output may not go to the high impedance state. (2) The C-element circuit has four transistors, but this structure has three transistors.

3. Proposed Novel DET-FF

Present day, the main goal of the researchers is to achieve small area, low power, and high speed in the field of VLSI designing. Therefore, several approaches have been considered by the researchers in VLSI applications to achieve these motives. We have designed a low-power glitch-free novel dual edge triggered flip-flop circuit design, as shown in Figure 5. Existing DET-FF designs [10–12] are designed by using only the C-element circuits. In the proposed design, we have used 2P-1N three-transistor structure with the combination of C-element circuit.

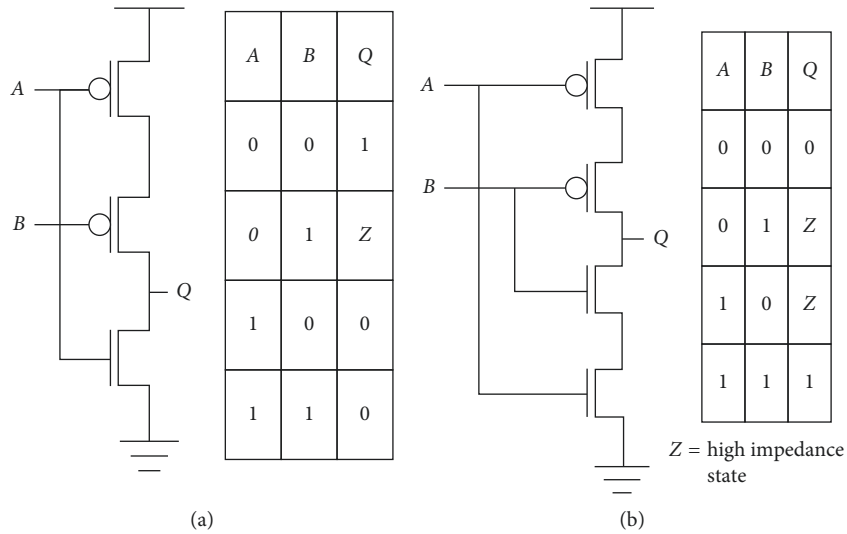

Figure 4: (a) 2P-1N structure and its truth table. (b) C-element circuit and its truth table.

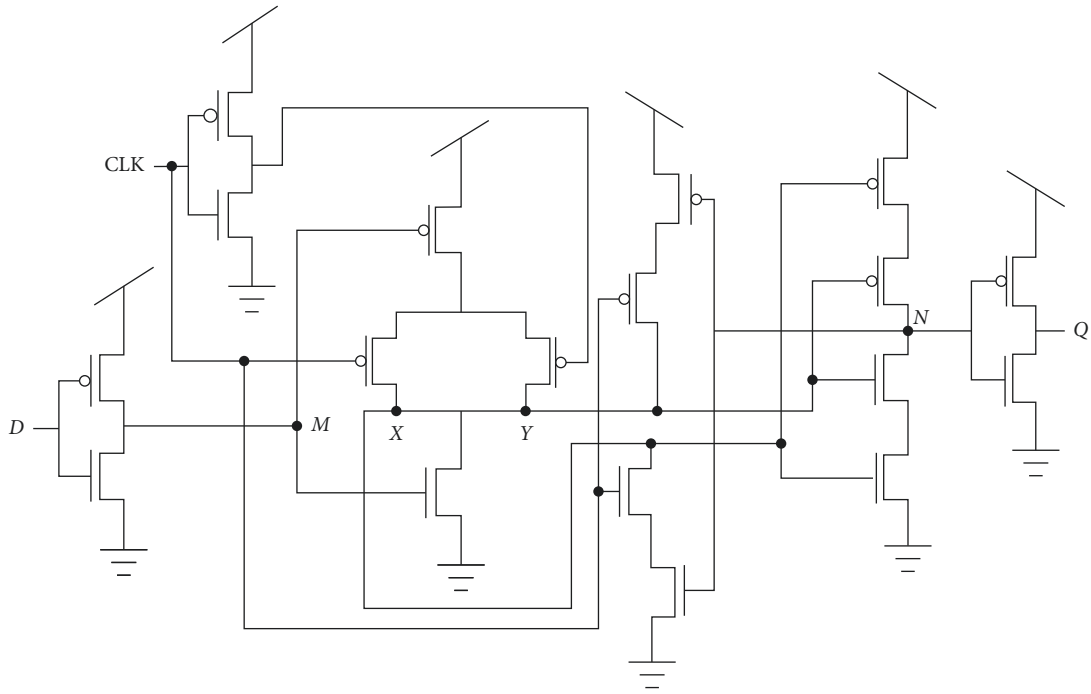

Figure 5: Proposed design with 2P-1N structure and C-element circuit.

Consequently, we have presented a novel robust low-power glitch-free dual edge triggered flip-flop design by mixed combination of 2P-1N and C-element structures which can work accurately at low power supply and provides the totally glitch-free output which can increase the system efficiency. The proposed circuit model consumes less power and provides glitch-free output. The working of the proposed design is as follows: case 1, the glitch either filter out or propagate to the output node Q; case 2, if glitch propagates to the output node Q, then it is filtered out through the feedback path. We just explain how this design avoids the glitches which may occur at the input node from the preceding combinational circuits.

Initially, let the nodes M and N be $M = 0$, $N = 0$, $X = 1$, and $Y = 1$, and the output be $Q = 1$ and clock **clk = 0**. At the node M, if any glitch occurs from the preceding combinational circuit, then the value of the node M will be changed from 0 to 1. Now for the first 2P-1N structure, the inputs are $M = 1$ and clk = 0, so for this input combination its output becomes $X = 0$. For the second 2P-1N structure, the inputs are $M = 1$ and clk = 1, so for this input combination its output becomes $Y = 0$. Thus, for the C-element circuit, input combination becomes $X = 0$ and $Y = 0$; therefore, C-element circuit's output switches to its input values, then $N = 0$, and the final output becomes $Q = 1$. Consequently, we can see that there is no change in the output state.

Now, let the nodes M and N be $M = 1$, $N = 1$, $X = 0$, and $Y = 0$, and the output be $Q = 0$ and clock **clk = 0**. At the node M, if any glitch occurs from the preceding combinational circuit, then the value of the node M will be changed from 1 to 0. For the first 2P-1N structure, the inputs are $M = 0$ and clk = 0; therefore, its output becomes $X = 1$. For the second 2P-1N structure, the input combination becomes $M = 0$ and clk = 1, and for this input combination, its output goes to the high impedance state; therefore, its output is in its previous state, that is, $Y = 0$. Now for C-element circuit, the input combination becomes $X = 1$ and $Y = 0$; therefore, its output goes to the high impedance state means its output is in its past state, that is, $N = 1$, and then output becomes $Q = 0$; consequently, again we can see that there is no change in the output state.

Now, let the nodes M and N be $M = 0$, $N = 0$, $X = 1$, and $Y = 1$, and the output be $Q = 1$ and clock **clk = 1**. At the node M, if any glitch occurs from the preceding combinational circuit, then the value of the node M will be changed from 0 to 1. Now, for the first 2P-1N structure, the inputs are $M = 1$ and clk = 1, so for this input combination, its output becomes $X = 0$. For the second 2P-1N structure, the inputs are $M = 1$ and clk = 0, so for this input combination, its output becomes $Y = 0$. Thus, for the C-element circuit, input combination becomes $X = 0$ and $Y = 0$; therefore, C-element circuit's output switches to its input values, then $N = 0$, and the final output becomes $Q = 1$. Consequently, again there is no change in the output state.

Now, let the nodes M and N be $M = 1$, $N = 1$, $X = 0$, and $Y = 0$, and the output be $Q = 0$ and clock **clk = 1**. At the node M, if any glitch occurs from the preceding combinational circuit, then the value of the node M will be changed from 1 to 0. For the first 2P-1N structure, the inputs are $M = 0$ and clk = 1, and for this input combination, its output goes to the high impedance state; therefore, its output is in its previous state, that is, $X = 0$. For the second 2P-1N structure, the input combination becomes $M = 0$ and clk = 0, and for this input combination, its output becomes $Y = 1$. Now, for C-element circuit, the input combination becomes $X = 0$ and $Y = 1$; therefore, its output goes to the high impedance state which means that output is in its past state, that is, $N = 1$, and then the final output becomes $Q = 0$; consequently, again there is no change in the output state. Thus, the faulty input value is left out without any cost in area, power, and time. Therefore, the proposed unique glitch-free novel dual edge triggered flip-flop design is completely glitch-resistant and has high speed and high efficiency.

4. Results and Analysis

The proposed low-power glitch-free novel dual edge triggered flip-flop design is performed through the SPICE simulator with Predictive Technology Model (PTM) 22 nm CMOS technology [15] with a power supply of 1 V. The channel lengths of all of the transistors are fixed to 22 nm. To simulate the circuit, the temperature is set to 27°C and the clock frequency is fixed to 500 MHz.

In the higher technologies, the operating voltage decreases and the frequency increases. Therefore, we have taken 1 V operating voltage, and the frequency is fixed to 500 MHz. When the operating frequency is high enough, the output will not reduce. The glitch-free novel dual edge triggered flip-flop design is simulated through the SPICE simulator, and the results are calculated and verified. The performance evaluation results are reported in Table 1. We note that the glitch-free novel dual edge triggered flip-flop design has a small number of transistors, the lowest average power consumption, the lowest power delay product (PDP), and the lowest propagation delay as compared to existing dual edge triggered flip-flop designs. Consequently, the proposed glitch-free novel dual edge triggered flip-flop design has high speed and high efficiency in comparisons with existing dual edge triggered flip-flop designs.

Table 1: Result analysis of different dual edge triggered flip-flops.

DET-FFs	Reference [10]	Reference [11]	Reference [12]	Proposed design
$P_{\text{avg. cons.}}$ (μw)	8.094	7.825	8.988	3.049
$t_{p(D\text{-}Q)}$ (ps)	72.872	65.536	84.297	26.995
$t_{p(\text{CLK-}Q)}$ (ps)	55.021	43.213	63.281	25.896
PDP (fJ)	0.589	0.513	0.758	0.082
Number of transistors	28	38	28	18

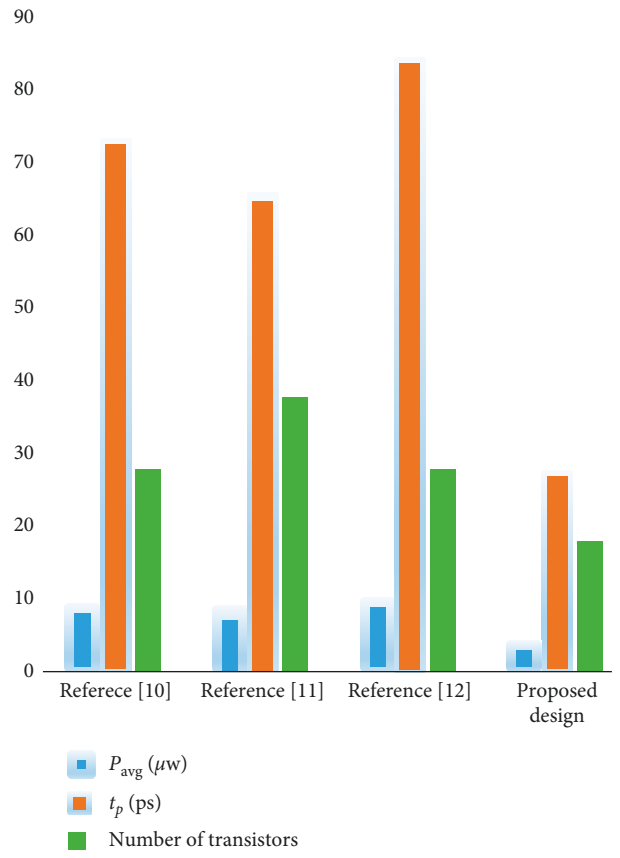

Figure 6: Power, delay, and area comparisons of different DET-FF designs.

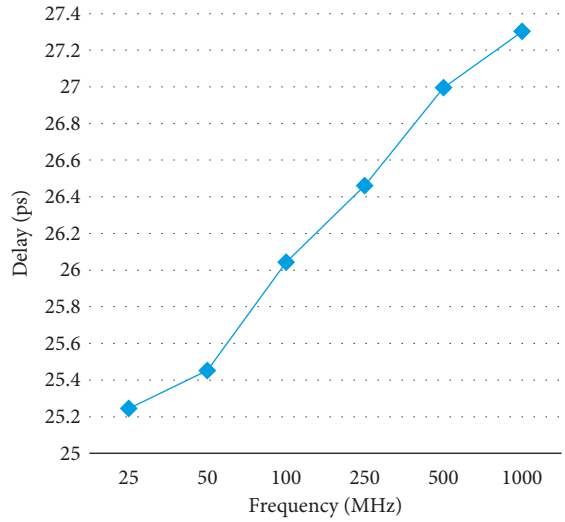

Figure 7: Delay analysis of proposed DET-FF design with different frequencies.

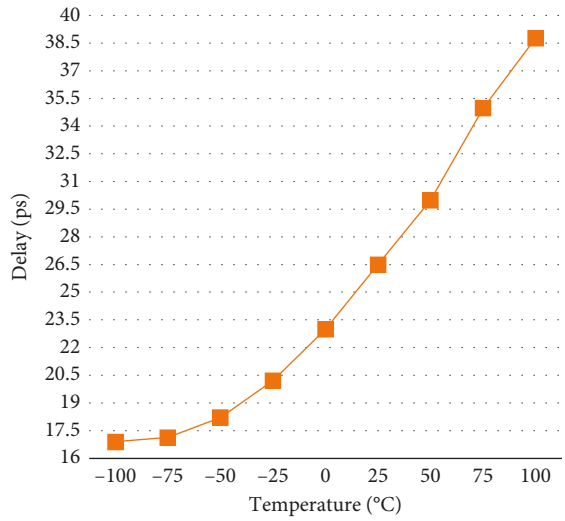

Figure 8: Delay analysis of proposed DET-FF design with different temperatures.

Comparative analysis of average power consumption, propagation delay, and area (number of transistors) for different glitch-free dual edge triggered flip-flop designs are shown in Figure 6, which reports that the proposed novel circuit design has the lowest average power consumption, the smallest area, and lowest propagation delay in comparison with other existing dual edge triggered flip-flop designs.

The propagation delay analysis of glitch-free novel dual edge triggered flip-flop is presented in Figures 7 and 8 with different parameters. The propagation delay increases with the frequency increment (from 25 MHz to 1000 MHz), as indicated in Figure 7. To reduce the delay, we should increase power supply voltage but in higher technology (22 nm) the power supply voltage decreases and the frequency increases, and consequently, delay increases with the frequency increment.

Due to the power supply voltage reduction, power consumption decreases but propagation delay increases. The propagation delay increases with the increase in the temperature (from −100°C to +100°C), as indicated in Figure 8. A higher temperature will decrease electrons and holes mobility and threshold voltage also; therefore, delay increases with the increase in the temperature.

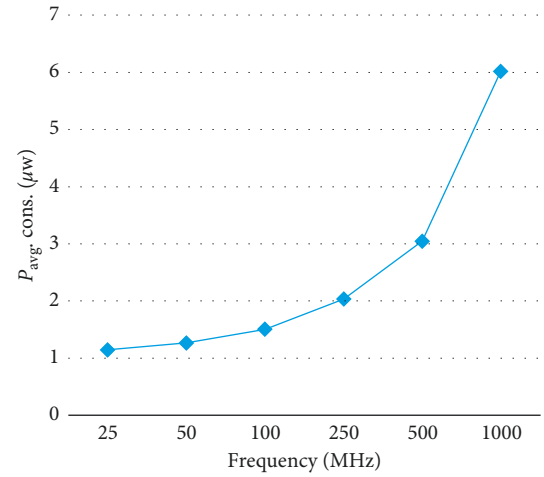

Figure 9: Average power consumption analysis of the proposed DET-FF design with different frequencies.

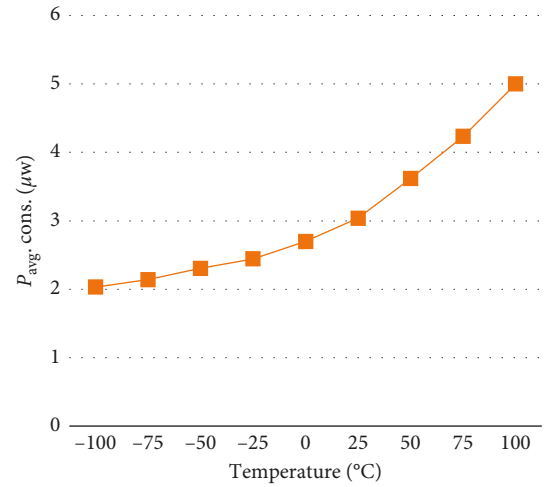

Figure 10: Average power consumption analysis of the proposed DET-FF design with different temperatures.

The average power consumption analysis of glitch-free novel dual edge triggered flip-flop is presented in Figures 9 and 10. Due to the propagation delay increment, the average power consumption increases with the frequency increment (from 25 MHz to 1000 MHz), as indicated in Figure 9. Here also, due to the propagation delay increment, the average power consumption increases with the temperature increment (from −100°C to +100°C), as indicated in Figure 10.

5. Conclusion

We have presented a low-power glitch-free novel dual edge triggered flip-flop which is designed with the mixed combination of 2P-1N and C-element structures. The glitch-free

novel dual edge triggered flip-flop design is the novel and unique design because it is constructed by using two fault resistant structures. If any glitch affects one of the structures, then it is corrected by the other structure. The glitch-free novel dual edge triggered flip-flop provides the totally glitch-free output and can increase the system efficiency. The presented novel design can reduce the 50% power consumption and contribute to the total system power savings. By using the fault resistant structure and internal dual feedback structure proposed design obtained robust and static operation. To reduce the input loading, the two structures are merged to share transistors connected with the data input. The proposed glitch-free novel dual edge triggered flip-flop has the lowest power consumption and lowest power delay product (PDP) as compared to the existing dual edge triggered flip-flop designs [10–12]. The proposed design has the smallest number of transistors and consequently occupies a small area and has the lowest propagation delay, thus providing high speed and high efficiency. To compare the novel design with existing designs, we have set 1 V power supply voltage and a system clock frequency of 500 MHz, and the proposed design was implemented with 22 nm CMOS technology and simulated through the SPICE simulator.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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