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Research Article

An Ultra-Low Power Parity Generator Circuit Based on QCA Technology

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Quantum-dot cellular automata (QCA) technology is one of the emerging technologies that can be used for replacing CMOS technology. It has attracted significant attention in the recent years due to its extremely low power dissipation, high operating frequency, and a small size. In this study, we demonstrate an *n*-bit parity generator circuit by utilizing QCA technology. Here, a novel XOR gate is used in the synthesis of the proposed circuit. The proposed gate is based on electrostatic interactions between cells to perform the desired function. The comparison results demonstrate that the designed QCA circuits have advantages compared to other circuits in terms of cell count, area, delay, and power consumption. The QCADesigner software, as widely used QCA circuit design and verification, has been used to implement and to verify all of the designs in this study. Power dissipation has been computed for the proposed circuit using accurate QCAPro power estimator tool.

1. Introduction

The continuous scaling down of CMOS-based devices in size, over the past few decades, in accordance with Moore's law leads to many different and difficult challenges as recently these devices are becoming more resistant to scaling [1–3]. One of the biggest challenges faced by transistor-based circuits is power consumption from leakage current due to the increased threshold voltage and decreased supply voltage [4]. The search for new technologies led to quantum-dot cellular automata (QCA) which has appealing features such as lower energy consumption and less cell density [5]. QCA designs offer lower energy and area solutions to the existing CMOS logic [6, 7]. QCA-based designs are suitable for fabrication of nanoscale devices. In QCA, circuits are fabricated by quantum cells, and each cell contains four quantum dots as well as two electrons. Quantum dots are nanoscale structures which are constructed from semiconductors such as InAs and GaAs. Transferring information is achieved by propagation of a polarization state instead of current in QCA implementation. This new technology attracted lot of researchers due to its direct use in quantum computing. Up to date, several works have been realized for the design of QCA logic circuits such as multipliers, adder, reversible ALU, divider, decoder, and memory circuits [8–15]. Many of these designs have advantages like faster speed and smaller size over their CMOS counterparts. In contrast, the mass production of ultra-small size QCA technology is very difficult. Additionally, QCA technology is prone to high error rates. The high error rate of this technology compared to traditional CMOS technology is due to the bridge, displacement, misalignment, and cell omission defects as well as stuck-at-fault which are likely occurred in the gates and interconnections. Defects can take place in both the chemical synthesis phase and the deposition phase. During the chemical synthesis phase, the QCA cells are manufactured, and during the deposition phase, the QCA cells are placed on a substrate. However, defects are more likely to occur in the deposition phase in which perfectly manufactured cells are imperfectly attached to the substrate. QCA devices are also susceptible to transient faults which are caused by thermodynamic effects,

radiation, and other effects, such as the energy difference between the ground and the excited state is small.

In this framework, the exclusive-OR gate is probably a vital part of complex digital circuits since it is often operated as structural blocks in digital fabrication. It can be used in the development of specific communication circuits such as parity generator and checker. QCA is one of the important technologies that enable high performance circuit design with low power consumption features. In this context, the exclusive-OR gate presents an important component. Various QCA-based exclusive-OR gates have been proposed in the literature, which have been designed using the majority gate-based methodology. In order to reduce power consumption and hardware complexity, this study presents an optimized QCA exclusive-OR gate, by which any complex digital designs may be synthesized. Additionally, an optimized parity generator circuit is achieved by using the proposed XOR gate. The main contributions of the paper are as follows:

(i) An efficient design of QCA exclusive-OR gate is proposed

(ii) The 4-, 8-, 16-, and 32 -bit QCA parity generator circuits are designed using this proposed gate as a building block

(iii) The designed circuits are simulated with QCADesigner software

(iv) Power dissipation of the proposed designs has been estimated

The rest of the paper is organized as follows: In Section 2, the backgrounds of QCA technology are reviewed. In Section 3, our proposed exclusive-OR gate is presented and compared to the conventional exclusive-OR gates. In Section 4, parity generator circuits are designed by using the proposed gate, and are compared to other counterpart designs. The simulation results of the proposed designs have been presented in Section 5. Finally, Section 6 concludes the paper.

2. Background of QCA

The basic functional block of QCA is the quantum cell that consists of four quantum dots. Each dot can hold one electron [6]. Electrostatic repulsions among the two electrons in the quantum cell make sure that the electrons can only reside in the antipodal sites. Thus, these electrons assume stable states, called polarizations, which are energetically equal and interpreted as binary "0"and"1" [16]. They have respective polarizations as $P =$ "−1" (logic "0") and $P =$ "+1" (logic "0") as shown in Figure 1. Polarization of the cells is calculated from equation (1) [17].

$$P = \frac{(\rho_1 + \rho_3) - (\rho_2 + \rho_4)}{\rho_1 + \rho_2 + \rho_3 + \rho_4}, \quad (1)$$

where ρ_i shows the electric charge at the i th point. Binary information is displayed using the position of two electrons in each logical cell.

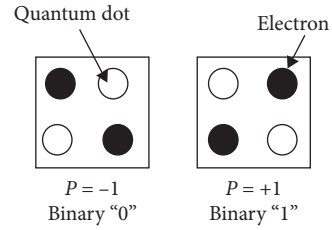

Figure 1: Two different polarizations of the quantum-dot cell.

On the other hand, to ensure that proper data flow takes place, QCA circuit clocking is introduced [18]. QCA-based circuits have a four-phased clocking namely switch, hold, release, and relax as illustrated in Figure 2. These four phases are generated by the traveling electric field wave perpendicular to the QCA plane. The various clock zones are represented by four different colors. Clock zero is represented by green, clock one by pink, clock two by blue, and clock three by white. Each clocking zone has a phase shift of 90 with respect to the adjacent ones. Each cell in a clocking zone behaves as latch [19].

Furthermore, when placed close to each other, the polarization of one QCA cell influences the polarization of the other, again by Coulomb interaction. One can exploit this effect in order to construct logic gates, such as the NOT and the MAJ gates. The inverter is the result of placing the cells such that their vertices are touching as illustrated in Figure 3(a) [20]. A majority voter is made up of five cells: one device cell (center cell), three inputs, and an output cell as depicted in Figure 3(b). The majority voter is driven by three input drivers A, B, and C. Its output can be computed as follows:

$$\mathrm{MV}(a, b, c) = AB + BC + AC. \quad (2)$$

Crossover types provide an advantage in circuit design in QCA as it offers a certain amount of design flexibility. QCA technology has two types of crossover. One, multilayer crossover and the other is coplanar crossover as depicted in Figures 4(a) and 4(b), respectively [16, 21]. The multilayer crossover yields high cost due to fabrication issue. In the second technique, two wires are overlapped in a similar plane to facilitate a simple binary wire cross an inverter chain.

3. Related Works

3.1. Previous QCA Exclusive-OR Circuits. Up to date, a widespread study in QCA has been outlined to achieve exclusive-OR designs [22–27] which are used in many of the digital logic circuits such as error detection circuits, arithmetic logic circuits, multiplexers, full adders, and comparators. The XOR gate is composed of two inputs and one output. Its output is true when two input operands are not the same, and the output is false otherwise.

In [22], the authors have proposed a novel low-power XOR gate. This designed gate consists of 13 cells and 0.012 μm^2 area. It occupies less area among the others. This

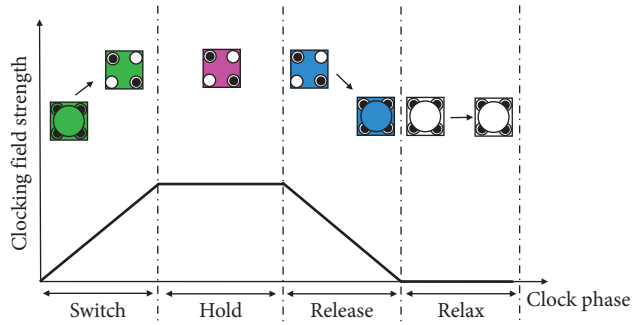

Figure 2: QCA clock zones.

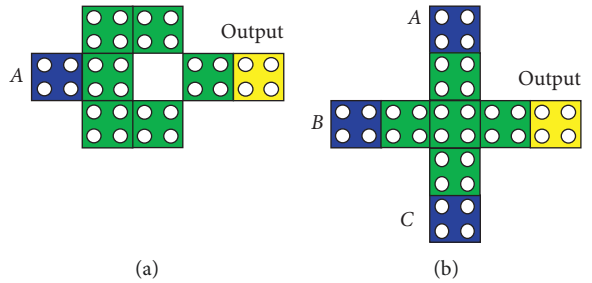

Figure 3: Inverter gate (a) and majority gate (b).

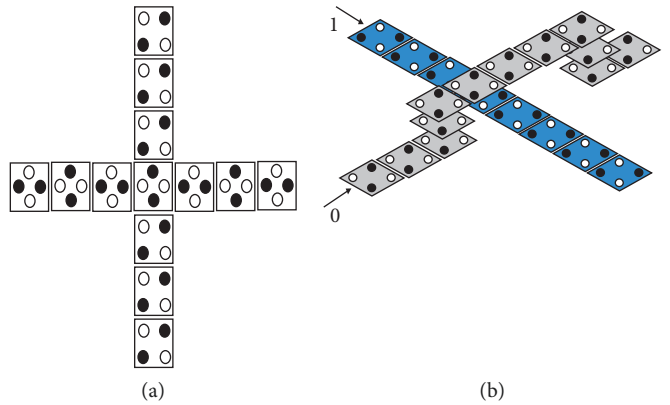

Figure 4: Signal crossover schemes. (a) Coplanar crossing. (b) Multilayer crossing.

design is based on the interaction between cells for implementing the desired function. It does not include any crossover in its structure. In addition, there is no any majority gate, which leads to less number of cells and power consumption. In [23], the authors have presented a novel, robust exclusive-OR gate. This designed gate consists of 28 cells and 0.02 μm^2 area. It is implemented without using any coplanar and multilayer crossover. This novel exclusive-OR design approach uses one five-input majority gate and two fixed polarization cells. The authors in [24] proposed a layout with 36 cells, extent 0.030 μm^2, and delay 0.75. This design is developed using a structure of coupled majority voter minority gate (CMVMIN), two majority gates, and two inverter gates. The design proposed in [25] requires 37 QCA cells, extent 0.030 μm^2, and delay 1. This design has an important number of cells and provides a large area. Also, a novel design of the XOR gate has been proposed by Bahar et al. in [26]. This design has achieved a reduction in the number of used cells and area consumption. It consists of 12 QCA cells, 0.02 μm^2 extent, and 1.25 delay. Figure 5 shows some previous designed exclusive-OR gates.

3.2. Proposed QCA Exclusive-OR Gate. In this section, a new efficient exclusive-OR gate is proposed by employing arranged and interacted QCA cells. The designed circuit and its simulation results are shown in Figures 6(a) and 6(c), respectively. Here, no majority gates are used to achieve the proposed design. The QCADesigner software is

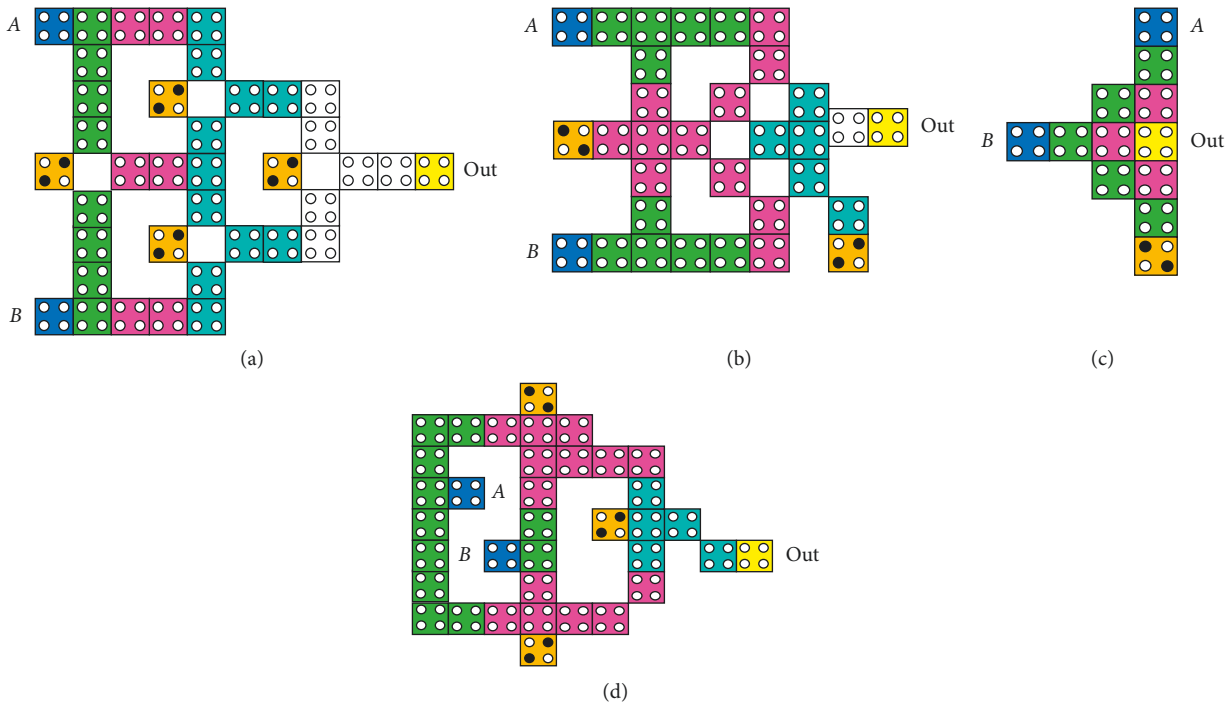

Figure 5: Exclusive-OR gates: (a) design in [24], (b) design in [27], (c) design in [26], and (d) design in [23].

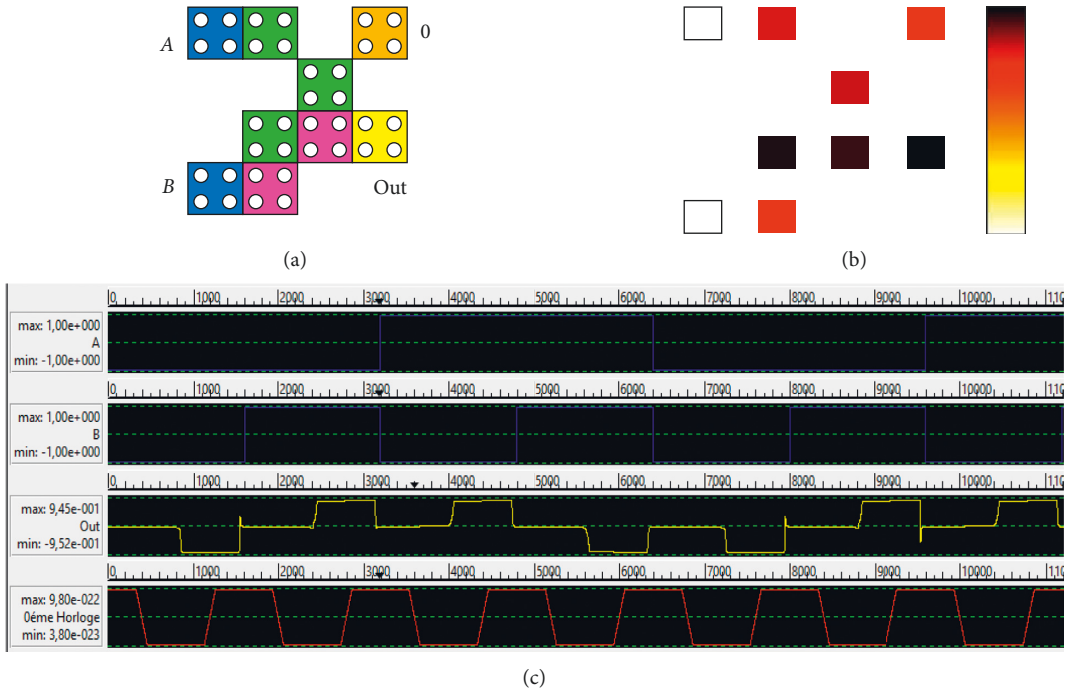

Figure 6: QCA layout of the designed (a) XOR gate, (b) power map, and (c) simulation outcomes.

used to verify the functionality of the designed circuit. The proposed QCA design covers only 9 cells, extent 0.01 μm^2, and a delay of 0.5. In contrast, the QCA layout proposed in [25] require 37 cells, extent 0.03 μm^2, and a delay of 1. Consequently, the designed XOR gate has an improvement of 75.67%, 66.66%, and 50% in terms of cell complexity, extent, and delay, correspondingly, compared with the design in [25]. In addition, the proposed gate attains an advancement of 67.85%, 50%, and 33.33% in terms of cell intricacy, area, delay, and cost, respectively, compared with

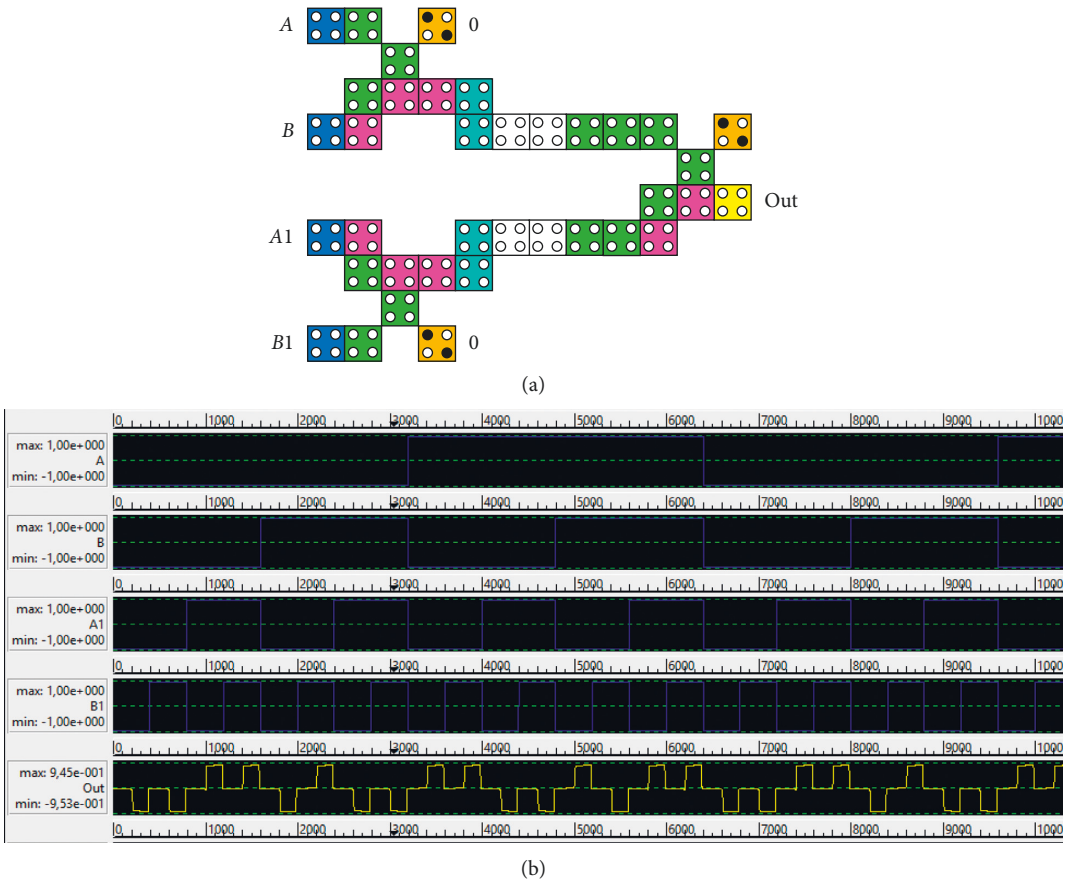

Figure 7: QCA layout of the designed (a) 4 bit parity generator and (b) simulation outcomes.

the design in [23]. Thus, the proposed gate can lead to QCA digital designs with less hardware complexity and power consumption.

4. Parity Generator Designs

The logic parity generator is a fundamental component for information processing chips and computing systems, in which the accurate matching of all received and transmitted data needs to be verified. It plays an important role in the design of digital circuits. As a result, several attempts have been done to implement this important logic component, especially in the QCA technology [22, 23, 25, 27]. In this section, we propose a novel QCA circuit for the parity generator. Figure 7(a) shows the proposed logic block implementation of the proposed 4 -bit parity generator circuit with three copies of the proposed QCA XOR gate. Figure 7(b) shows the simulation results of the proposed 4 -bit parity generator circuit. The timing diagram indicates that the parity output is correctly obtained. It should be noted that this circuit can be easily extended to the n-bit QCA parity generator circuit. Figure 8 shows QCA implementation of the proposed 8 -bit parity generator circuit. In this focus, we demonstrate only the QCA layouts of 4- and 8 -bit parity generator circuits because of the lack of space. Here, the cell count, area, and delay of the designed 4- and 8 -bit parity generator circuits are considerably improved compared to 4- and 8 bit parity generator circuits in [22, 23, 25].

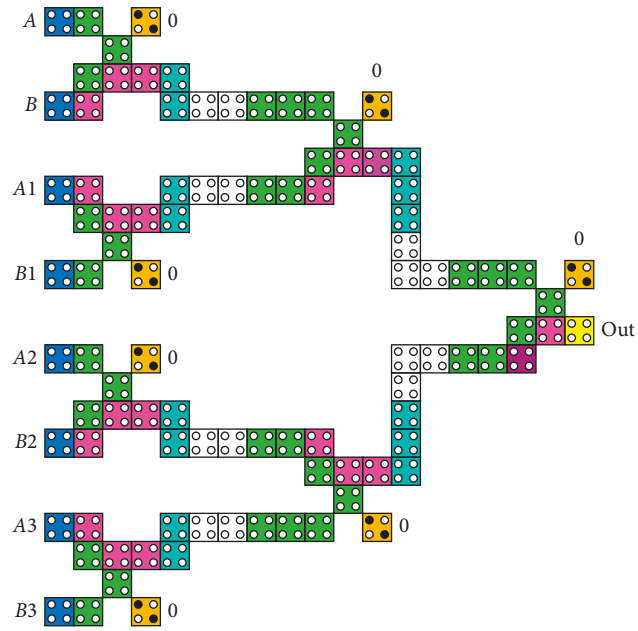

Figure 8: QCA implementation of the proposed 8 bit parity generator circuit.

5. Simulation Results and Comparison

The QCADesigner tool version 2.0.3 is used to verify the functionality of the designed QCA circuits. The utilized parameters for the simulation are as follows: cell width = 18 nm, cell height = 18 nm, dot diameter = 5 nm, number of samples = 12.800, convergence tolerance = 0.001, radius of effect = 80 nm, relative permittivity = 12.9, clock high = $9.8E-22$J, clock low = $3.8E-23$J, clock amplitude factor = 2, layer separation = 11.5 nm, and maximum iterations per sample = 100. Table 1 shows the comparison results of the proposed exclusive-OR gate with previously reported XOR gates. The comparison is carried out considering the cell count and total area as well as latency of the circuit. As can be seen from Table 1, the proposed XOR circuit has less number of cells and reduced device area in comparison with the existing circuits. In Table 2, the proposed parity generator circuits have been compared with previously reported parity generator circuits [23, 25, 28–30]. Clearly, our designs outperform the proposed designs in [23, 25, 28–30]. In this work, QCAPro software [31], a probabilistic designing engine, has been applied for the energy depletion study. The power dissipation map of the proposed XOR gate is depicted in Figure 6(b). According to Figure 6(b), the darker cells exhibit higher average power dissipation and white squares represent the input cells. Table 3 illustrates the power consumed by the proposed QCA XOR design. The estimation is performed at temperature $T = 2$ K by employing three channeling energy levels, namely, $0.5E_k$, $1.0E_k$, and $1.5E_k$. As is shown in Figure 9, our proposed gate has the lowest energy dissipation value at three separate tunneling energy levels as compared with the circuits in [22, 23, 25, 27, 32]. Consequently, the use of the proposed XOR gate in the design of parity generator circuits will provide more power savings. It is noticeable from Figure 10 that, our proposed architectures have least energy dissipation value in diverse sizes (4, 8, 16, and 32 bits) compared to existing ones.

The power consumption of the proposed circuits is analyzed with the Hartree-Fock approximation [33]. The Hamiltonian matrix of a mean-field approach is explained as

$$H = \begin{bmatrix} \frac{-E_k}{2}\sum_i C_i f_i, j & -\gamma \\ -\gamma & \frac{E_k}{2}\sum_i C_i f_i, j \end{bmatrix} = \begin{bmatrix} \frac{-E_k}{2}\left(C_{j-1} + C_{j+1}\right) & -\gamma \\ -\gamma & \frac{-E_k}{2}\left(C_{j-1} + C_{j+1}\right) \end{bmatrix}. \quad (3)$$

The kink energy cost of two neighboring cells i and j with opposite polarizations is derived as follows:

Table 1: Comparison of the proposed exclusive-OR gate with the previous work.

Circuit	Cell count	Area (μm^2)	Clock no.cycle	Crossover type
XOR [28]	60	0.09	1.5	Coplanar
XOR [29]	54	0.08	1.5	Coplanar
XOR [30]	67	0.06	1.25	Coplanar
XOR [25]	37	0.03	1	Not required
XOR [24]	36	0.03	0.75	Not required
XOR [23]	28	0.02	0.75	Not required
XOR [22]	13	0.012	0.5	Not required
XOR [22]	12	0.011	0.5	Not required
Proposed XOR	9	0.01	0.5	Not required

Table 2: Comparison results of parity generators.

Circuit	No of bits	Cell count	Area (μm^2)	Clock no.cycle
[28]	4	187	0.32	2.75
	8	465	0.92	4
	16	1024	2.41	5.25
	32	2220	5.96	6.5
[29]	4	168	0.28	2.75
	8	408	0.8	4
	16	912	2.09	5.25
	32	1968	5.16	6.5
[30]	4	188	0.2	2.25
	8	369	0.49	2.25
	16	847	1.46	3.25
	32	1862	3.58	4.25
[25]	4	111	0.14	2
	8	269	0.43	3
	16	603	1.13	4
	32	1,312	2.81	5
[23]	4	87	0.10	1.75
	8	213	0.30	2.75
	16	480	0.81	3.75
	32	1,044	2.08	4.75
Proposed design	4	37	0.05	1.5
	8	97	0.18	2.5
	16	227	0.50	3.5
	32	511	1.3	4.5

Table 3: Power dissipation analysis of the XOR gate.

QCA circuit	Dissipation of power $T = 2.0$ K		
	$\gamma = 0.5E_k$	$\gamma = 1E_k$	$\gamma = 1.5E_K$
XOR [25]	46.99	66.54	89.51
XOR [27]	47.28	62.39	80.34
XOR [32]	39.06	53.63	71.08
XOR [23]	36.20	50.28	66.58
XOR [22]	11.36	18.42	26.02
Proposed XOR	6.7	11.29	16.19

$$E_{i,j} = \frac{1}{4\pi\varepsilon_0\varepsilon_r}\sum_{n=1}^{4}\sum_{m=1}^{4}\frac{q_i q_j}{\left|r_i - r_j\right|}. \quad (4)$$

For any instance, the power depletion of a QCA cell can be calculated as follows:

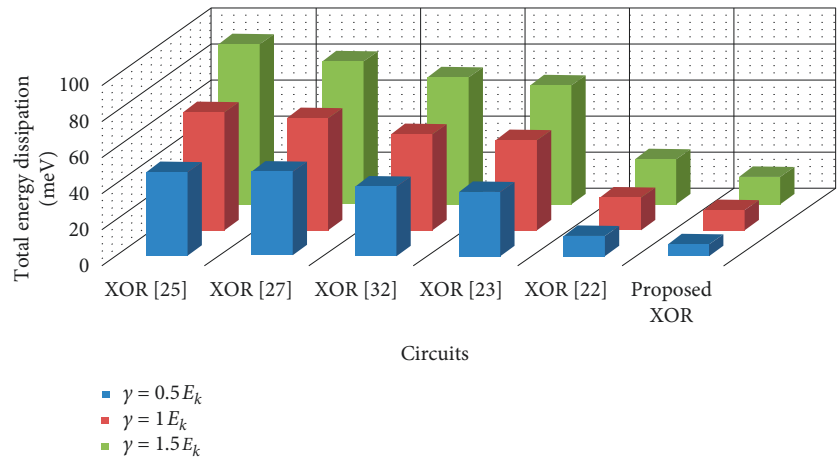

Figure 9: The total power dissipation of the presented XOR gate at three different tunneling energy levels ($T = 2$ K).

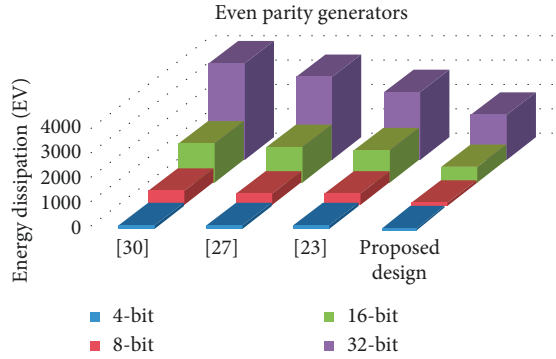

Figure 10: Power dissipation comparison between different size (4-, 8-, 16-, and 32-bit) parity generator designs.

$$P_{\text{Total}} = \frac{\mathrm{d}}{\mathrm{d}t}E = \frac{\overline{h}}{2}\left(\frac{\mathrm{d}}{\mathrm{d}t}\overrightarrow{\Gamma}\right)\cdot\overrightarrow{\lambda} + \frac{\overline{h}}{2}\overrightarrow{\Gamma}\left(\frac{\mathrm{d}}{\mathrm{d}t}\overrightarrow{\lambda}\right) = P_1 + P_2. \tag{5}$$

6. Conclusion

Quantum-dot cellular automata (QCA) is an upcoming nanoscale technology with great prospect to provide compact circuits with low energy consumption compared to CMOS technology. In this paper, a novel design of exclusive-OR gate in the QCA technology has been presented. It is more preferable for QCA implementations, since it does not use any rotate cells and majority gates. It incredibly reduces the area. Even parity generator circuits were designed and analyzed using this proposed gate as a building block. The designed circuits were simulated and verified by using the QCADesigner tool version 2.0.3. The power dissipation of the proposed designs has been investigated using QCAPro tools. A comparison of various XOR gates and parity generator circuits with regards to cell count, area, and energy dissipation is analyzed in this paper. The comparison results show that the designed QCA circuits have significant improvement compared to other existing ones.

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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