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Research Article

A 1.25–12.5 Gbps Adaptive CTLE with Asynchronous Statistic Eye-Opening Monitor

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The equalization of a large attenuation signal and multirate communication in high-speed serial interface is hard to balance. To overcome this difficulty, an adaptive equalization system with optimized eye-opening monitor is proposed. The designed eye-opening monitor is based on the asynchronous statistic eye diagram tracking algorithm, and the eye diagram is obtained by undersampling with the low-speed asynchronous clock. With the eye-opening monitor into the adaptive loop, an adaptive equalization system combined with continuous-time linear equalization (CTLE) is completed. And the inductor peaking technology is used to improve the capacity of compensation. With SMIC 28 nm CMOS process to achieve the overall design, the power consumption and core chip area are 12 mW @ 12.5 Gbps and 0.12 mm^2, respectively. And postsimulation results show that it can offer compensation from 6 to 21 dB for 1.25–12.5 Gbps range of receiving data, which achieves a large range of data rate and channel loss, and its power efficiency is 0.046 pJ/bit/dB for the worst case, which is better than most previous works.

1. Introduction

High-speed serial interface has become the inevitable choice for high-speed data transmission. However, the nonideal factors of the wireline transmission channel will lead to channel noise and frequency attenuation and significantly reduce the quality of the received signal. Various equalization techniques had been used to compensate the loss, among the most popular are decision feedback equalizer (DFE) and CTLE. The DFE can eliminate intersymbol interference (ISI) effectively, but it will increase system complexity, and for high-speed data, the time constraint is apparent. On the contrary, CTLE can realize the compensation of the full-frequency band and has simple structure, and it does not need any clock signal. For that reason, we choose the CTLE to realize the signal equalization.

In addition, a fixed preset equalizer may not work well across a large range of data rate, it is imperative to have the robust adaptation algorithm to achieve a well-behaved adaptive equalizer. The adaptive equalization algorithm based on energy extraction proposed by Won et al. [1] had good compensation effect on high-speed data, but the circuit complexity and power consumption were greatly increased through its algorithm. Choi et al. [2] used the frequency filter to change low-frequency gain adaptively, and the adaptive linear device had a simple circuit structure, but the frequency information shaped by the rectifier was inaccurate, and the stability still needed to be optimized. The data pattern information also had been used to change the equalization coefficient in [3], which had better area and power efficient, but the compensation capacity was limited.

As the optimal compensation for the high-frequency signal and low-frequency signal is difficult to balance, and it is even more difficult to cover a large range of channel loss. In order to overcome these obstacles, we proposed an optimized adaptive equalization system which is based on

eye diagram tracking. We use the asynchronous undersampling method to obtain an on chip eye-opening monitor. And the proposed tolerance judgement in the adaptation algorithm could track the change of the data rate, and it can avoid the over equalization results. Besides, the undersampling method alleviates the circuit timing constraints and simplifies the circuit design, and we use the active-inductor technology to improve the performance of the CTLE module. The optimized CTLE combined with the digital eye-opening monitor realizes the automatic equalization for channel changing, and it also can achieve the optimal compensation results for different data rates. The equalization system can compensate the data rate range from 1.25 Gbps to 12.5 Gbps and provide a wide equalization range from 6 dB to 21 dB. And the power efficiency of the core circuit is only 0.046 pJ/bit/dB. It achieves both design flexibility and stability, also with lower power consumption.

2. Nonideal Factors of Channel

The nonideal characteristics of transmission channels mainly include skin effect, dielectric loss, return loss, crosstalk, and all kinds of noises. Among which, the skin effect and dielectric loss are main reasons for high-frequency channel losses [4, 5]. Their impacts can be expressed by

$$C_S = \exp\left[\left(-h_s * l\right)(1 + j)\sqrt{f}\,\right], \tag{1}$$

$$C_d = \exp\left[\left(-h_d * l\right)f\right], \tag{2}$$

where h_s and h_d are the coefficients of skin effect and dielectric loss, respectively, f is the frequency, and l is the transmission distance. It indicates that skin effect loss and dielectric loss are both proportional to the channel length. And when the signal frequency is relatively low, the channel attenuation is mainly resulted from the skin effect. With signal frequency increasing, the attenuation caused by the dielectric loss becomes more and more obvious. Taking these nonideal factors into account, we can get the frequency response trend of the actual channel, shown in Figure 1. The actual channel shows low-pass characteristics and suppresses the high-frequency signal significantly.

3. Adaptive Equalization Algorithm

3.1. Asynchronous Statistic Eye Diagram Tracking Algorithm. Figure 2 shows two eye diagrams and their statistic results. According to the actual eye diagram, it can be concluded that height of the eye-opening indicates the amplitude of the received signal. In addition, the thickness of the eyelid proves that if the loss signal gets an effective and uniform compensation after passing through the equalization system. With that observation, the eye diagram can be obtained by two steps: sampling and counting. The asynchronous undersampling technique is adopted to achieve eye diagram sampling [6], in which the sampling

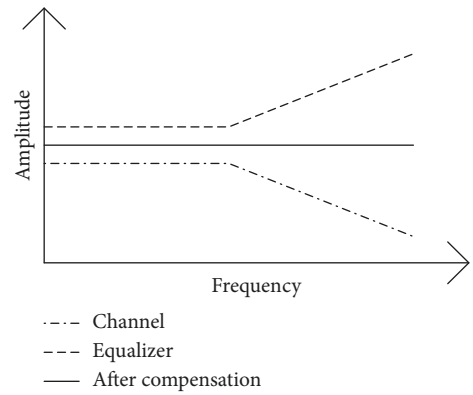

Figure 1: Channel frequency characteristic.

clock is not synchronous with the periodic input signal and the sample clock is much slower than the data clock. As shown in Figure 3, the asynchronous clock is used to sample the high-speed input signal, and the low-frequency clock is sweeping the sample time across the period of the input waveform. After a certain number of sampling periods, the time domain waveform of input data can be obtained, and the statistical result of sampling data represents the information of input data. In that way, we would realize an on-chip eye-opening monitor. And certain eye characteristics can be extracted as long as a sufficient number of samples are taken.

However, the adaptive algorithm in [6] has a defect that the analysis of the statistic information is not comprehensive enough. Using comparison of Figures 2(a) and 2(b) to explain that, it seems that biggest sample number of Figure 2(b) is much bigger than Figure 2(a). But when we focus on the compensation performance, in fact, Figure 2(b) provides an over equalization, and Figure 2(a) gets the optimal equalization result, which proves that simply searching for the histogram that has the largest peak value to choose the equalization coefficient is not accurate. In others words, not only the height of eye opening shows the amplitude of the compensated signal, the reference voltage value corresponding to the maximum value of statistics results provides useful information too. Therefore, we optimize the algorithm with a tolerance judgement, using the reference voltage to do the second-order decision. The proposed optimized algorithm could further improve the performance of the adaptation system and gets the optimal equalization effects.

3.2. Architecture of Adaptive Equalizer. Figure 4 presents the structure of the proposed adaptive equalizer, which mainly consists of a CTLE, a full differential dynamic comparator, and a DAC to provide reference voltage, and Figure 5 demonstrates the adaptation control flow chart. Based on the asynchronous undersampling technique, we divide the amplitude of an eye diagram into 16 reference levels, named REF_j (j = 0, 1, 2, . . ., 15), and the equalizer coefficients are called EQ_i (i = 0, 1, 2, . . ., 15), which aims to provide a large range of equalization capacities.

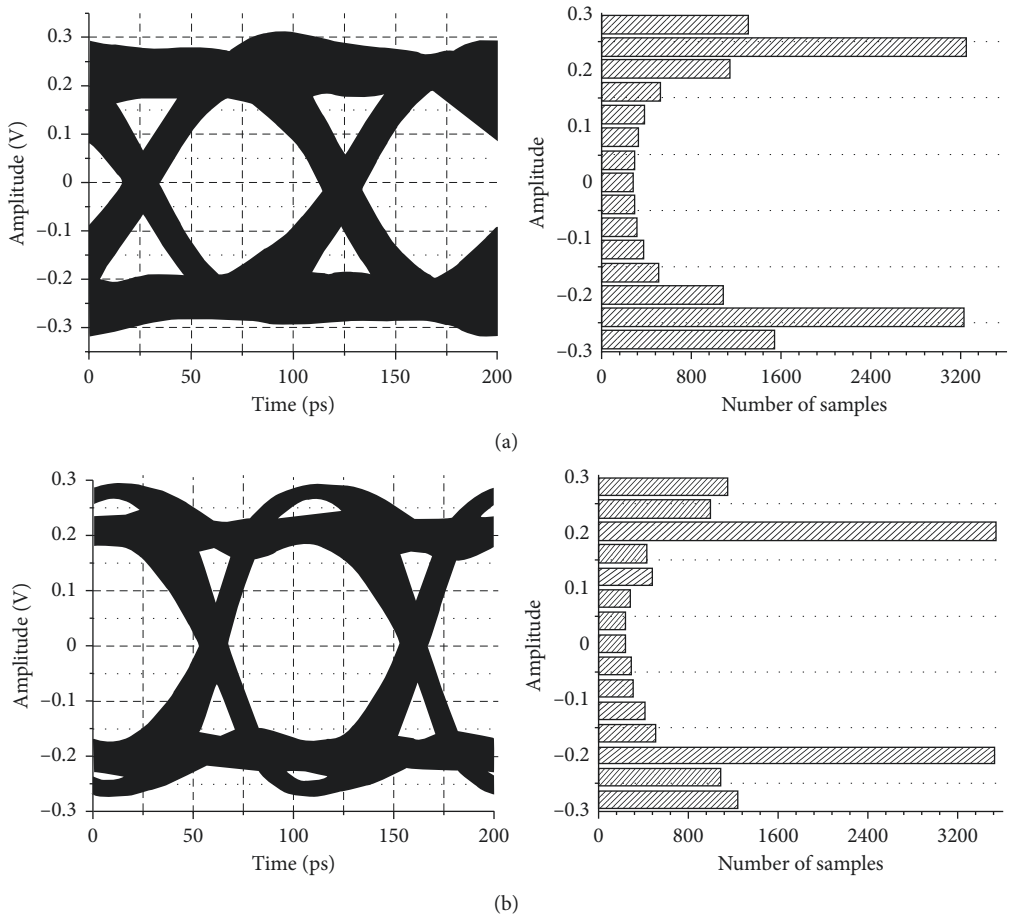

Figure 2: Eye diagrams and statistic bars. (a) Optimal equalization. (b) Over equalization.

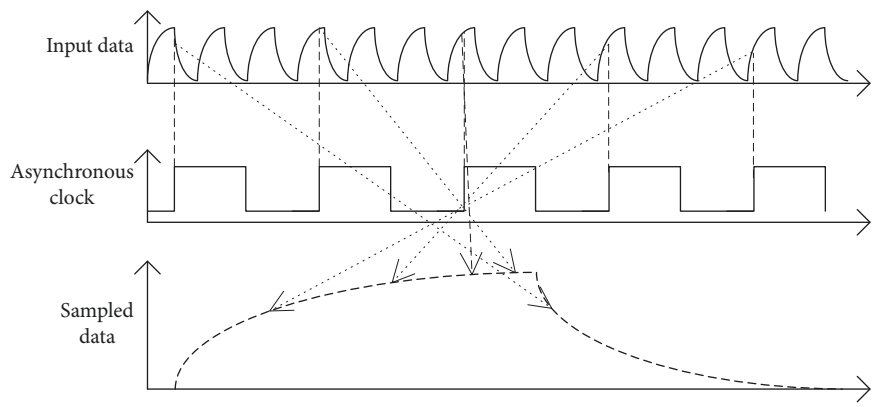

Figure 3: Asynchronous undersampling technique.

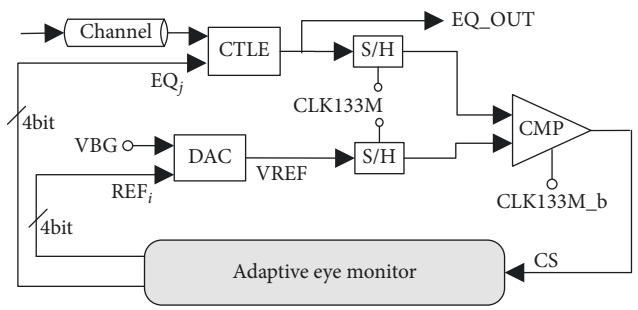

Figure 4: Proposed adaptive equalizer structure.

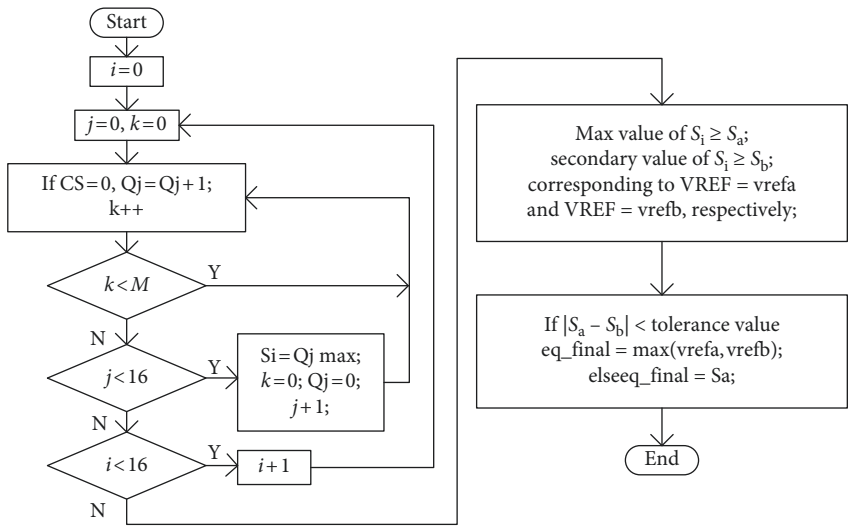

Figure 5: Proposed adaptive equalizer structure's adaptation control flow chart.

The operation process of the adaptive equalization system is as follows: Step 1, the adaptive eye-opening monitor sets the original equalization coefficient as EQ_0, the reference level is set to REF_0, and then DAC outputs the corresponding reference voltage VREF. Step 2, the full differential comparator compares equalized data EQ_OUT with VREF in M (for example, $M = 8192$) CLK sampling periods (k is the count number of sample clocks). And the comparison result CS is transmitted to the eye-opening monitor. Step 3, the eye-opening monitor moves the reference value to next level ($j = j + 1$) and repeats sampling operation in Step 2, until $j = 15$, and the whole eye diagram corresponded to EQ_0 is sampled. Step 4, change the equalization coefficient to EQ_1 and repeat operation in Step 2 and Step 3, and those processes are repeated for each equalization coefficient ($i = 0, 1, 2, \ldots, 15$). Then, the eye-opening monitor obtains the counting results in order to complete the eye diagram. Step 5, the eye-opening monitor selects the optimal coefficient of the equalizer and completes the adaptive process.

The algorithm provides a full consideration of asynchronous statistic eye diagram tracking. In Step 5, the eye-opening monitor firstly selects the biggest and secondary peaking value of eye diagram statistical results, which are S_a and S_b, respectively. And they both correspond to a reference voltage (called $vref_a$ and $vref_b$), which indicate the amplitude of eye diagram. If the difference value of S_a and S_b is less than the tolerance value, then it compares the reference voltages $vref_a$ and $vref_b$ and chooses the equalization coefficient corresponding to the bigger reference voltage. The tolerance value is depends on comparator and sampler errors, and we did the simulation of those circuits to set the tolerance value.

The settle time of the proposed adaptation process is calculated by M (sample number) × 16 (reference voltage level number) × 16 (equalization coefficient number) × 7.5 ns (asynchronous clock period)~15 ms.

4. Implementation of Equalizer System

The system consists of a CTLE with the active inductor, a full differential dynamic comparator, and a DAC. We use a digital circuit to achieve the algorithm to improve design flexibility and, meanwhile, promote system performance and algorithm efficiency.

4.1. CTLE. The common structure of conventional CTLE is capacitive degenerated differential pair [7], as shown in Figure 6(a). The transfer function is given by

$$H(s) = \frac{(g_m R_d)(1 + sR_sC_s)}{(1 + sR_sC_s + (g_m R_s/2))/(1 + sR_dC_d)}, \quad (3)$$

where g_m is the transconductance of input difference pairs. And the expressions for the locations of zero and poles can be deduced as $w_z = 1/(R_sC_s), w_{p1} = (1 + g_mR_s/2)/R_sC_s, w_{p2} = 1/(R_dC_d)$.

This topology, however, suffers from limited bandwidth and consequently insufficient compensation at high frequencies. It is because w_{p1} exceeds w_z by a factor of $(1 + g_mR_s/2)$, and the DC gain drops by the same amount of factor. In other words, g_mR_s must stay low so as to avoid large DC loss (otherwise the interposed buffers suffer). This issue limits the maximum achievable boost in magnitude and phase. To expand the bandwidth of CTLE, the inductor peaking technology is introduced, shown in Figure 6(b). The transfer function of CTLE with the inductor load is given by

$$H(s) = \frac{g_mR_d}{1 + (g_mR_s/2)} \cdot \frac{1 + (s/w_{z1})}{1 + (s/w_{p1})} \cdot \frac{1 + (s/w_{z2})}{1 + (2\zeta/w_n)s + (s^2/w_n^2)}, \quad (4)$$

where $w_{z2} = 2\zeta w_n, \zeta = (R_d/2)(C_d/L_p)^{1/2}, w_n = 1/(C_d \cdot L_p)^{1/2}$ and w_{z1} and w_{p1} are unchanged.

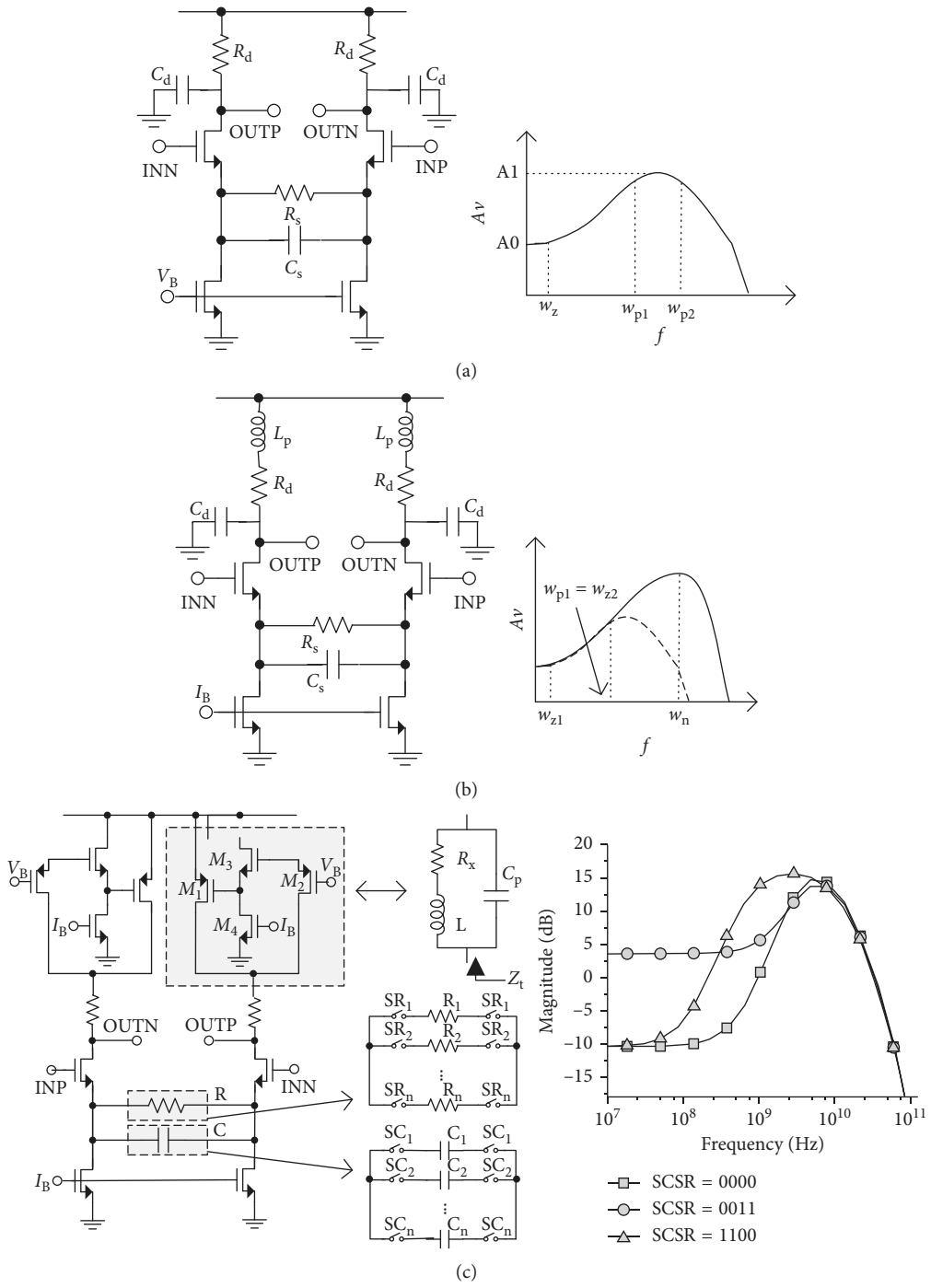

Figure 6: CTLE circuit. (a) Conventional CTLE circuit and frequency-response curve. (b) CTLE with inductor peaking. (c) Designed CTLE circuit and frequency-response curve.

Since a passive inductor may take large area, we introduce an optimized structure of CTLE called the active inductor to realize the inductive termination [8, 9], which aims to extend the output bandwidth in the presence of large capacitive loads and save chip area. A PMOS-based active-inductor circuit is used as the load of CTLE in Figure 6(c), which enhances the compensation ability for high-speed data. It uses a MOS resistor (M2, which operates in deep-triode region) through which the output node is coupled to the gate of the PMOS transistor M1. A level shifter, consisting of a source follower M3 and a current source M4, is inserted between M1 and M2 to allow a lower gate bias

voltage for M1. The termination impedance of presented CTLE is given by the following equation:

$$Z_t = \frac{1 + j\omega C_{gs} R_2}{(g_{ds} + g_m) - \omega^2 R_2 C_{ds} C_{gs} + j\omega\left(C_{gs} + C_{ds} + R_2 C_{gs} g_{ds}\right)}, \tag{5}$$

$$\begin{aligned} L &= \frac{\left(R_2 C_{gs1}\right)}{(g_{ds1} + g_{m1})}, \\ C_p &= C_{ds1}, \\ R_x &= \frac{1}{(g_{ds1} + g_{m1})}, \end{aligned} \tag{6}$$

where C_{ds}, C_{gs}, g_{ds}, and g_m are the parameters of M1 and R2 is the equivalent resistor. And the termination impedance can be represented as (6).

The inductive peaking facilitates the equalizing filter design, and the 20 dB compensation for data rate above 10 Gbps becomes feasible. Besides, for a single transmission data rate, as the equalizer is designed for a fixed frequency point, the adjusting of the equalization coefficient only depends on the channel change. While the data rate is changing, it could not achieve an optimal compensation by a coefficient fixed equalizer. Therefore, the RC values both need to be changed through the switches SR and SC to provide different DC gains and peaking frequency. There are 4 resistance values (SR is 2 bit) and 4 capacitance values (SC is 2 bit), and they can combine out 16 sets of different equalization coefficients. The frequency response of designed active-inductor CTLE is shown in Figure 6(c). It can realize a compensation range of 6–21 dB in the effective frequency band, the DC gain can change from −10 dB to 5 dB, and the peaking frequency can scan from 1.25–12.5 GHz (at Nyquist frequency), which can provide an area-efficient alternative for passive inductive terminations and well satisfy the equalization ability.

4.2. Full Differential Comparator and DAC. The full differential comparator consists of the SA in the first stage, and the slave set-reset (SR) latch in the second stage is shown in Figure 7(a), and Figure 7(b) is the DAC circuit using partial pressure resistance structure and hot code control switch to reduce switch number.

5. Postsimulation Results

The equalizer layout in SMIC 28 nm CMOS technology is demonstrated in Figure 8, core circuit power consumption and area are 12 mW @ 12.5 Gbps and 0.12 mm^2, respectively, and the digital implementation is included.

The postsimulation results are shown in Figure 9. The S-parameter curve of a 563 mm PCB channel with 18.1 dB loss at 5 GHz is shown in Figure 9(a), and the eye diagram of the 10 Gbps receiving signal is shown in Figure 9(b); it can be seen that the eye diagram is closed totally. The acquired eye diagram after the adaptive equalizer of 456, 593, 336, and 1355 mm PCB channels are shown in Figures 9(c)–9(f), and according channel loss are −21.4 dB @ 6.25 GHz, −22.3 dB @ 5 GHz, −12 dB @ 5 GHz, and −8 dB @ 620 MHz, respectively. According data rates are 12.5 Gbps, 10 Gbps, 10 Gbps, and 1.25 Gbps, respectively. By comparing Figure 9(d) with Figure 9(e), it shows that, for the fixed data rate, while the channel length is changing, the equalization system can realize well equalization. And by comparing Figures 9(c) and 9(d) with Figure 9(f), it demonstrates that although the data rates are different, the loss data can achieve the optimal compensation results after the equalization system, and the changing of signal frequency can be well tracked by the proposed adaptation algorithm. And the final equalization coefficients for Figures 9(c)–9(f) are SRSC = 0000, 0001, 0110, 1111, respectively. On the one hand, it proves that the equalizer can provide large compensation range; on the other hand, it shows that the adaptation algorithm can avoid the over equalization results with the proposed eye-opening monitor. As seen from the results, receiving loss signal can be well compensated after equalization, and eye diagrams open well.

Compared with other recent work given in Table 1, the advantages of this design can be displayed intuitively. Comparing with the eye-opening monitor in [15], our design can compensate the bigger loss, and the adaptation part is realized on the chip. A proposed FOM is calculated by

$$\text{FOM} = \frac{\text{total power}}{\text{data rate} * \text{channel loss}}. \tag{7}$$

The proposed figure of merit normalizes the power consumption, transmission data frequency, and channel loss, which compares the system performance under the same evaluation index, and can make a more comprehensive measurement. And as shown in the comparison table, thanks to digital eye-opening tracking monitor and the asynchronous sampling technique, the FOM of proposed adaptive equalizer is clearly superior to other designs, which means that this design achieves better compensation ability for the same data rate, and it also has obvious advantage in power efficiency. The active-inductor peaking technology expands the compensation ability of the equalizer, which can achieve the signal frequency range from 1.25 Gbps to 12.5 Gbps, and channel losses range from −6 dB to −21 dB. In the meantime, the proposed optimized asynchronous statistic eye diagram tracking algorithm also ensures to obtain the appropriate compensation effects and avoids over equalization for the different data rate.

6. Conclusion

An adaptive equalization system based on the asynchronous statistic eye diagram tracking algorithm was realized on SMIC 28 nm CMOS technology. As the height of eye diagram and the concentration of statistical data are taking into account, the optimized adaptive algorithm provides a tolerance judgement to track equalized eye opening so that the equalization system can avoid under equalization or over equalization of different signal frequencies. The active-inductor peaking technology also enhances CTLE capacity to provide a wide equalization range. The adaptive equalization system can offer

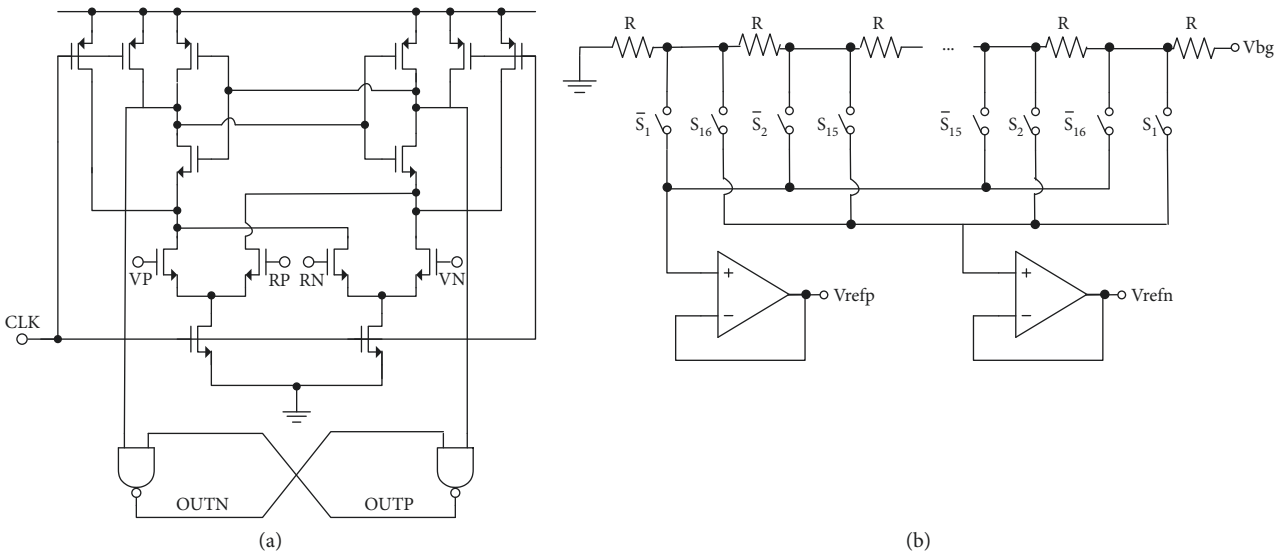

Figure 7: Circuit of full differential comparator and DAC.

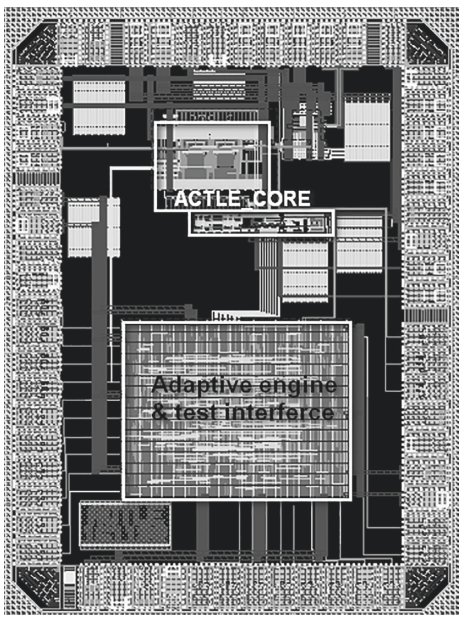

Figure 8: Layout of the chip.

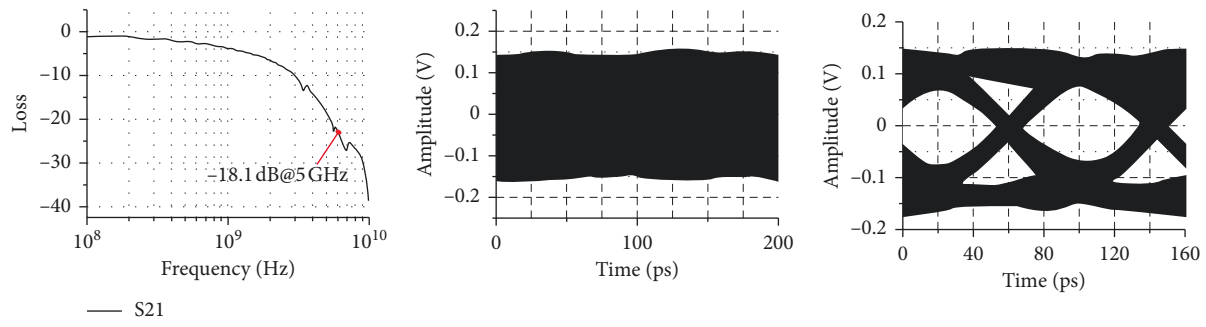

Figure 9: Continued.

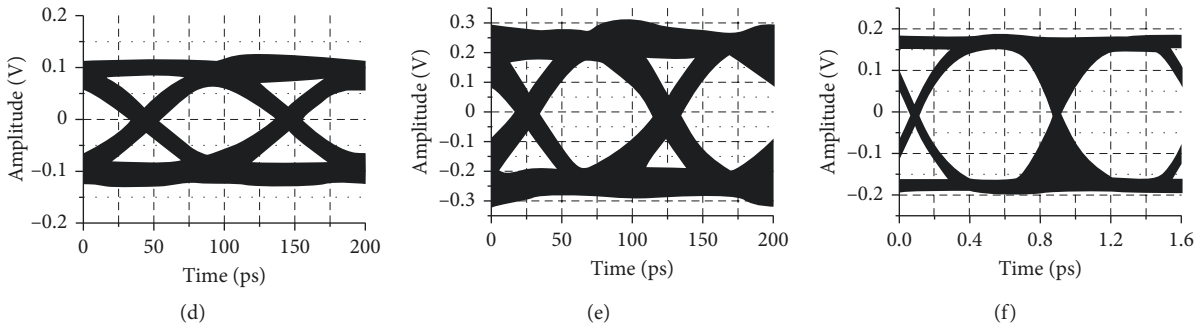

Figure 9: Postsimulation results of adaptive equalization for different data rates and channel losses.

Table 1: Performance comparison.

Reference	[10]	[11]	[12]	[13]	[14]*	[15]*	[6]*	This work
Technology	65 nm	65 nm	180 nm	130 nm	110 nm	90 nm	130 nm	28 nm
Equalization	DFE	CTLE + DFE	CTLE	DFE	CTLE + DFE	DFE	CTLE	CTLE
Adaptation	YES	YES	YES	NO	YES	YES	YES	YES
Data rate (Gb/s)	10	10	5	6.25	11.5	10	5.4	1.25–12.5
Channel loss (dB)	16.2	25	6.8	18	21.7	8.8	6–16	6–21
Supply (V)	1.2	—	1.8	1.2	1.3	1.2	—	0.9/1.8
Core area (mm^2)	0.01	—	—	—	0.014	0.01	0.18	0.12
Power (mW)	24	66	18	1.875	25.35	11	34.99	12
FOM (pJ/bit/dB)	0.148	0.264	0.53	0.167	0.102	0.125	0.405	0.046

*Measurement data and others are based on simulation.

a compensation from 6 dB to 21 dB for 1.25–12.5 Gbps of the receiving signal, and its power efficiency is 0.046 pJ/bit/dB for the worst case. It has low power consumption and strong adaptive capacity so as to greatly optimize the high-speed interface analog front-end design. As the adaptation judgement is realized by the digital controller, it achieves a reusable design of the adaptive equalization system as well.

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

Acknowledgments

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