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Research Article

A Low Leakage Autonomous Data Retention Flip-Flop with Power Gating Technique

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With the scaling of technology process, leakage power becomes an increasing portion of total power. Power gating technology is an effective method to suppress the leakage power in VLSI design. When the power gating technique is applied in sequential circuits, such as flip-flops and latches, the data retention is necessary to store the circuit states. A low leakage autonomous data retention flip-flop (ADR-FF) is proposed in this paper. Two high-V_{th} transistors are utilized to reduce the leakage power consumption in the sleep mode. The data retention cell is composed of a pair of always powered cross-coupled inverters in the slave latch. No extra control signals and complex operations are needed for controlling the data retention and restoration. The data retention flip-flops are simulated with NCSU 45 nm technology. The postlayout simulation results show that the leakage power of the ADR-FF reduces 51.39% compared with the Mutoh-FF. The active power of the ADR-FF is almost equal to other data retention flip-flops. The average state mode transition time of ADR-FF decreases 55.98%, 51.35%, and 21.07% as compared with Mutoh-FF, Balloon-FF, and Memory-TG-FF, respectively. Furthermore, the area overhead of ADR-FF is smaller than other data retention flip-flops.

1. Introduction

With the scaling of CMOS technology, leakage power has been continuously increasing and has been a major partition of the total power consumption. It is reported that more than 40% of total power can be due to the leakage currents [1–6]. In an idle circuit, leakage is the main source of power consumption. Therefore, for the battery-dependent portable devices, reducing the leakage is critical for a longer battery lifetime of those devices [3–8].

Many methods are proposed to suppress the leakage currents. Power gating is one of widely employed techniques that are available in VLSI design [9–11]. Power gating technique employs high-V_{th} sleep transistors between the low-V_{th} functional block and supply/ground rails. The circuit with power gating technique has two operating modes: active mode and sleep mode. In active mode, the sleep transistors connect the supply/ground rails and functional block to ensure the circuit working properly. During sleep mode, the idle leakage currents are suppressed by cutting off the connection [2, 6, 9, 12].

When the power gating technique is employed in sequential circuits, such as latches and flip-flops, the circuit states would be lost during sleep mode. Data retention function is essential for sequential circuits which need to restore the data after they are woken up and make sure that the correct data can be transferred to the output [5, 13].

Several data retention flip-flops with power gating technique have been proposed. A conventional MTCMOS flip-flop (Mutoh-FF) is proposed by Mutoh et al. in [8]; it is capable of preserving data but has a significant power overhead and a high circuit area overhead. The Balloon-FF is first proposed by Shigematsu et al. in [14], it preserves data during the sleep mode and reduces the standby power. However, it requires complex control signals to maintain and restore the circuit states during and after the sleep mode. The data retention flip-flop (DRFF) is proposed by Mahmoodi-Meimand and Roy in [3], it stores data in power-down

cross-coupled inverters. However, the inputs of the inverters should be properly gated using extra gating circuitries in the sleep mode. Henzler et al. propose a dynamic state retention flip-flop using fine-grained sleep transistor scheme. But the retention time is in the range of milliseconds [4]. The self-data retention flip-flop proposed by Seomun and Shin uses virtual power rail to control the operation. It removes wiring overhead caused by control signals in conventional data retention flip-flops. However, extra pulse generator and large PMOS switch are needed to speed up the operation mode transition [5]. The Memory-FF proposed by Jiao and Kursun in [6] uses a sleep signal to control the operation mode without extra control signals, thereby reducing the control complexity. However, when the Memory-FF enters and leaves the sleep mode, the sleep signal and clock signal should meet the timing requirement to ensure the correct operation. Moreover, the output node of the all proposed data retention flip-flops is floating in the sleep mode.

In this paper, a new low leakage autonomous data retention flip-flop with power gating technique is proposed. It has a significantly simplified control circuitry as compared with the previously published data retention flip-flops. The transition of active mode and sleep mode is controlled by a sleep signal, and no extra control signals are required. Moreover, the circuit overcomes the floating output in the sleep mode via always powered cross-coupled inverters.

The paper is organized as follows. Previous power gating data retention flip-flops are reviewed in Section 2, and the limitations of them are also presented. In Section 3, the proposed power gating data retention flip-flop is described. Simulation results and analysis are provided in Section 4. And the conclusions are offered in Section 5.

2. Previous Works Review

Power gating technique is an effective method to reduce the leakage in sequential circuits during standby mode [2, 5, 13, 15, 16]. Retaining the circuit state during the sleep mode is highly significant in power gating sequential circuits. This section reviews some well-known previous data retention flip-flops with power gating technique.

2.1. Mutoh Flip-Flop Circuit. The Mutoh-FF is first proposed by Mutoh et al. in [8]. As presented in Figure 1, high-V_{th} MOS devices are utilized in the master and slave latches, and along the critical path are low-V_{th} devices. Several sleep transistors are located within the Mutoh-FF.

The low-V_{th} devices along the critical path insure a high Clock-to-Q speed of the Mutoh-FF. Both PMOS and NMOS high-V_{th} devices are used to eliminate the sneak leakage paths during the sleep mode. The four employed high-V_{th} MOS switches result in a high area overhead and a significant power overhead of the operation mode transition. When the sleep signal and clock signal transition low, the flip-flop enters the sleep mode. The recent data is sampled by the cross-coupled inverters (I3 and I5) and maintained during the whole sleep mode, as shown in Figure 1. The sleep signal turns high before the clock is enabled at the end of sleep mode, so that the data retention cell restores the data to slave latch.

2.2. Balloon Flip-Flop Circuit. Another low leakage data retention flip-flop (Balloon-FF) is proposed in [14], as shown in Figure 2. It is composed of high-V_{th} data retention cell (Balloon) and low-V_{th} master and slave latch. A centralized high-V_{th} NMOS sleep switch is shared by the low-V_{th} devices.

The critical path of Balloon-FF is similar to the Mutoh-FF and it ensures a high speed. The sleep switch is utilized to disconnect the low-V_{th} stages and the ground rails during the sleep mode. The Balloon-FF circuit area overhead is decreased compared with the Mutoh-FF, due to the fact that Balloon-FF circuit only employs one centralized NMOS sleep switch. However, two extra control signals $B1$ and $B2$ are required in Balloon-FF. And the two extra control signals must meet complex timing requirements as illustrated in Figure 3. The required complex data storage and recovery operations result in a high power overhead.

2.3. Memory-FF Circuit. There are two Memory-FFs proposed by Jiao and Kursun in [6]. One uses two high-V_{th} NMOS pass transistors for accessing the data retention cell (DRC), the other uses a pass transistor and a transmission gate for accessing the DRC. The memory flip-flop using the transmission gate (Memory-TG-FF) is presented in Figure 4. The master and slave stages and the high-V_{th} NMOS sleep transistor of the Memory-TG-FF are similar to that of the Balloon-FF. The data retention cell of Memory-TG-FF is different from that of Balloon-FF. Two high-V_{th} pass devices (TGpass and MN2 in Figure 4) are used to access the data retention cell. The required operation timing is shown in Figure 5.

The Clock-to-Q speed and area overhead of Memory-TG-FF are similar to those of Balloon-FF. The sleep signal is also used for controlling the data retention and restoration operations in Memory-TG-FF. The clock signal turns low when the circuit is during sleep mode. At the end of the sleep mode, the sleep signal turns high before the clock is enabled, as illustrated in Figure 5. The output node of the Memory-TG-FF is floating in the sleep mode.

3. The Proposed Autonomous Data Retention Flip-Flop

A new low leakage autonomous data retention flip-flop is presented in this section. The proposed autonomous data retention flip-flop (ADR-FF) with power gating technique is composed of master and slave stages which gated by PMOS and NMOS high-V_{th} transistors and an autonomous data retention cell (DRC) attached to the slave stage, as shown in Figure 6.

A high-V_{th} PMOS transistor and a high-V_{th} NMOS transistor are utilized to cut the connection of master and slave stages with the supply power and ground rails, in order to reduce the leakage during the sleep mode of ADR-FF. The low-V_{th} devices along the critical path of the ADR-FF insure a high Clock-to-Q speed. The only sleep signal is enough for

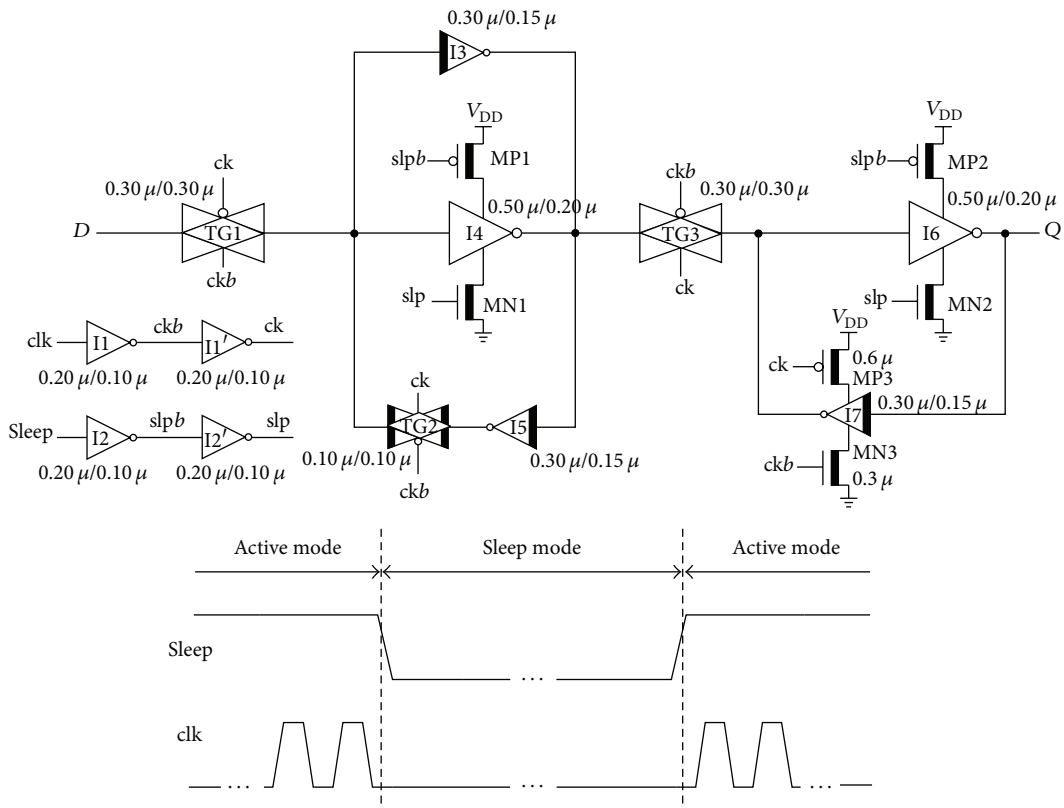

Figure 1: The Mutoh-FF circuits and its operation timing.

controlling the operation mode transition of the proposed ADR-FF. No extra control signals are required, so that the complexity of control timing is reduced significantly. The DRC is composed of cross-coupled inverters (I5 and I6). Moreover, the cross-coupled inverters conquer the problem of output floating when the sleep transistors are off.

In the active mode, the sleep signal keeps low, the sleep transistors (MP1 and MN1) are turned on, and the circuit works similar to a positive triggered D flip-flop. The cross-coupled inverters (I5 and I6) maintain the states of Q. The feedback path (TG4 and I7) keeps on and makes the states of node stable when the clock signal is low.

As soon as the sleep signal transfers low to high, the circuit turns into sleep mode, and then the sleep signal keeps high. The sleep transistors are all turned off, the master stage loses the connection with the power supply and ground rails, and the low-V_{th} devices except for I6 all stay off. Thus, the new data cannot be transferred to slave stage. The DRC maintains the circuit state at the end of active mode. Thereby, the power dissipation of ADR-FF is reduced in the sleep mode while keeping the presleep circuit state.

At the moment of sleep signal turning low, the ADR-FF enters into active mode. Since the presleep data kept in the output node Q in the sleep mode, there is no data recovery operation during the sleep mode to active mode transition. As shown in Figure 6, the operation transition of active mode and sleep mode is easily controlled. The simple operation timing saves significantly the active-sleep and sleep-active transition power.

Table 1: The sizes of sleep transistors with different data retention flip-flop circuits.

Flip-flops	Header (um)	Footer (um)
Mutoh-FF	2.0	1.0
Balloon-FF	/	1.0
Memory-TG-FF	/	1.5
ADR-FF	3.0	1.5

4. Simulation Results

The NCSU 45 nm PTM CMOS technology is used for the postlayout simulations of the circuits in this paper. The test bench in Figure 7 is applied to assure the fairness of the simulations. The buffers and the output loads are also the postlayout devices. To evaluate the performance of the different data retention flip-flops, the standard transmission gate flip-flop (ST-TG-FF) is also simulated. The schematic of ST-TG-FF is presented in Figure 8. The power dissipation, delay overhead, and the area overhead of the different flip-flops are all presented in the section.

The size of transistors in different circuits is shown in Figures 1, 2, 4, 6, and 8. Table 1 lists the size of sleep transistors

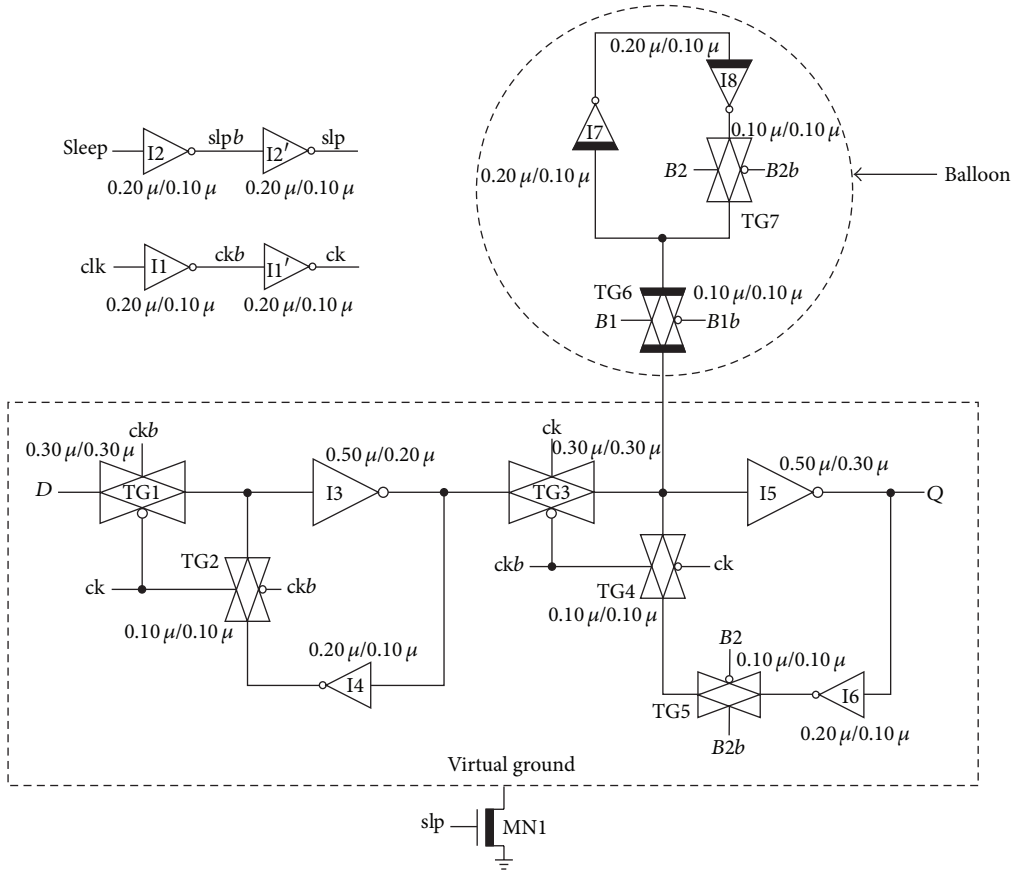

Figure 2: The schematic of Balloon-FF circuits.

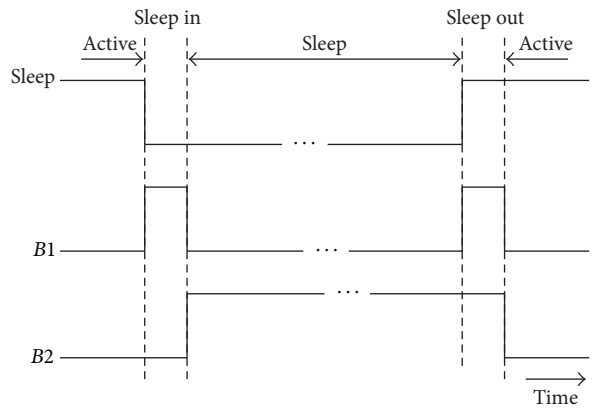

Figure 3: Sequence of the control signals for the Balloon-FF circuit.

utilized in the different circuits. The sleep transistors in Mutoh-FF cannot be shared due to the fact that they are utilized to reduce the sneak leakage current [16], while they are shared in Balloon-FF, Memory-TG-FF, and ADR-FF. The zero bias threshold voltage of transistors is shown in Table 2.

Table 2: The zero bias threshold voltages of transistors.

Transistors	NMOS		PMOS	
	Low-V_{th}	High-V_{th}	Low-V_{th}	High-V_{th}
V_{th0} (V)	0.471	0.853	−0.423	−0.771

4.1. The Operation of the ADR-FF Circuit. The operations of the ADR-FF in different modes are verified in this section. The simulation waveforms of the ADR-FF are illustrated in Figure 9. In the active mode, the ADR-FF operates similar to a standard positive edge trigged master-slave FF.

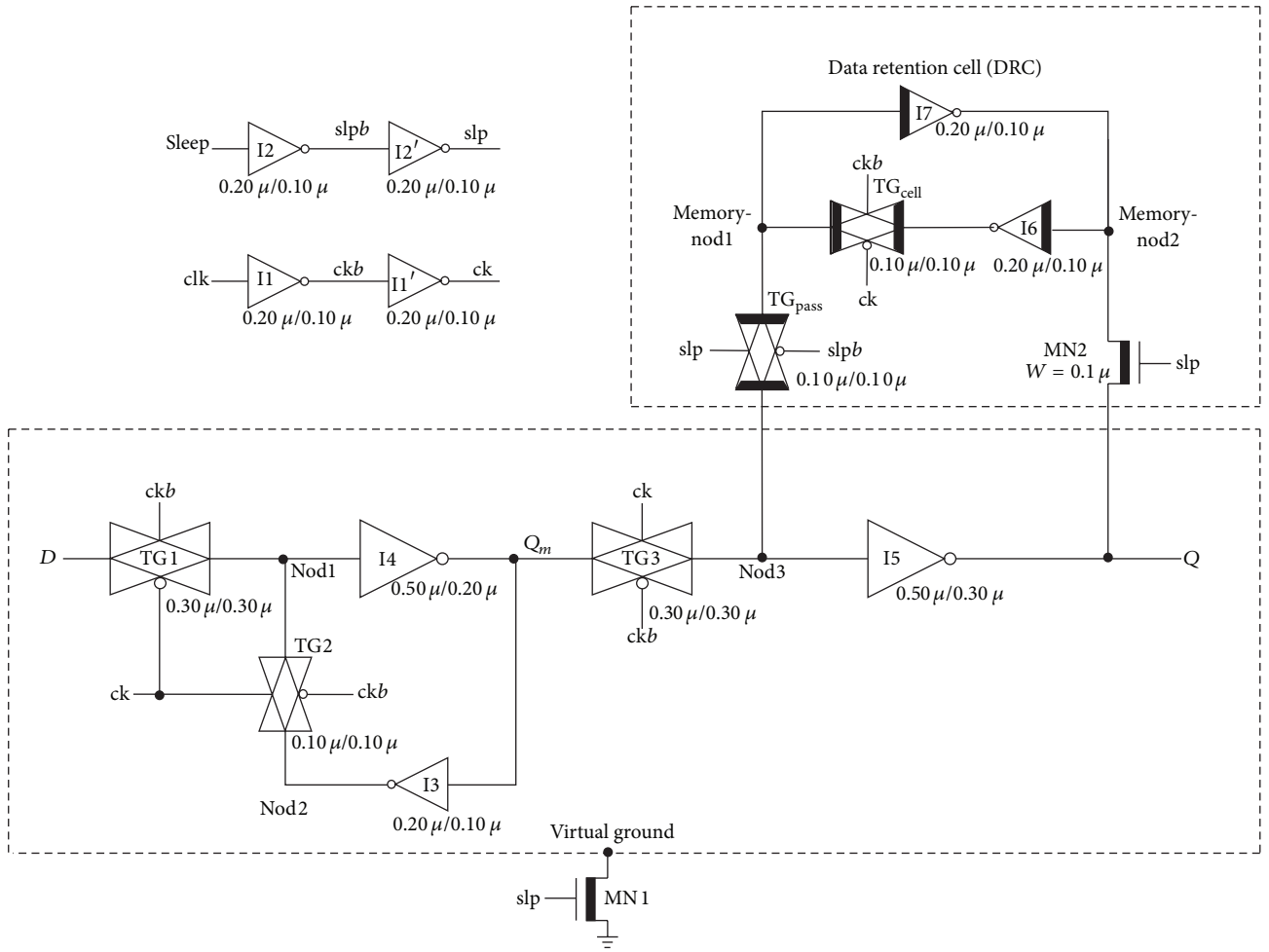

Figure 4: The schematic of Memory-TG-FF circuits.

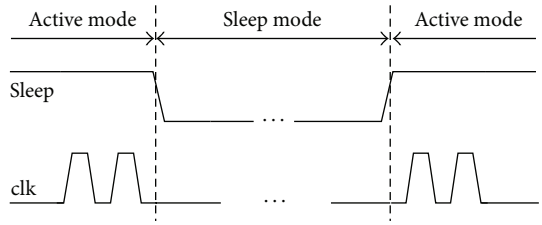

Figure 5: The operation timing of Memory-TG-FF.

The ADR-FF enters the sleep mode when the sleep signal transitions low to high. The waveforms representing the operations of storing a "0" and a "1" with the ADR-FF are shown in Figure 9. With the ADR-FF, the new data is not only transferred to Q but also stored in the data retention cell. Therefore, no additional data transfer operations are required for storing the data into the DRC before entering the sleep mode. When the ADR-FF is idle, the data that was last sampled by the DRC is maintained throughout the sleep mode.

At times t_1 and t_3, sleep signal goes high; the data "0" and "1" are stored in the DRC, respectively, as shown in Figure 9. Then the data is maintained in the output node Q during sleep mode.

The ADR-FF turns back to the active mode when the sleep signal transitions high. Since the presleep data is reserved in the output node Q, no additional data transfer operations are required for data recovering. Furthermore, the clock signal and sleep signal of the ADR-FF have not any timing requirements for storing and retrieving the circuit state to and from DRC while entering and leaving the sleep mode.

As is shown in Figure 9, the transition of active mode and sleep mode is controlled only by a sleep signal in the ADR-FF, and no extra control signals are required. As compared

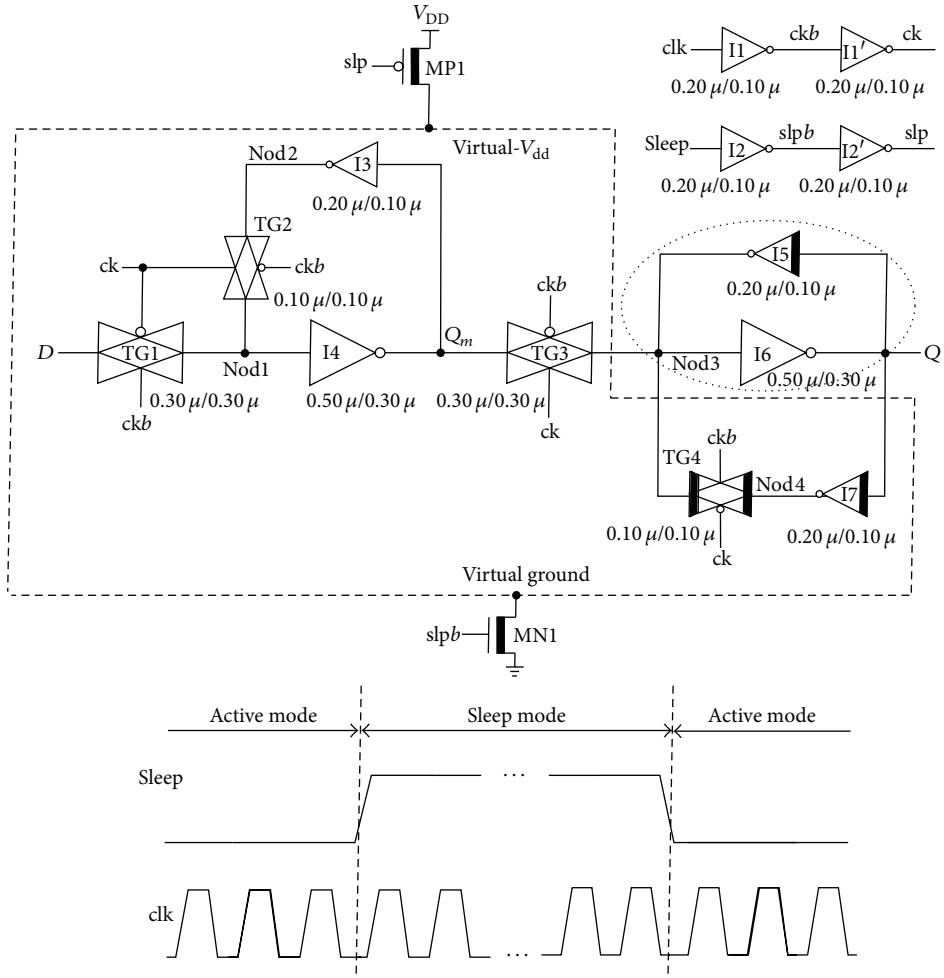

Figure 6: The proposed ADR-FF circuits and its operation timing.

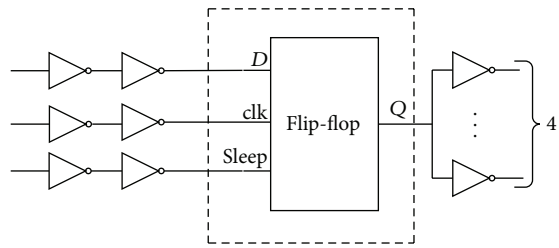

Figure 7: The test bench of the different data retention flip-flops.

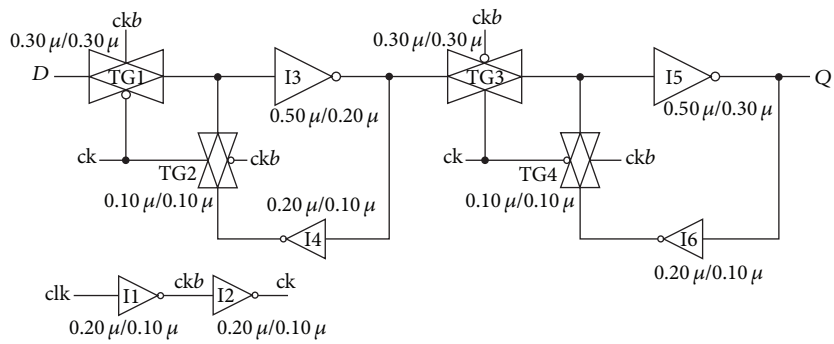

Figure 8: The schematic of ST-TG-FF circuits.

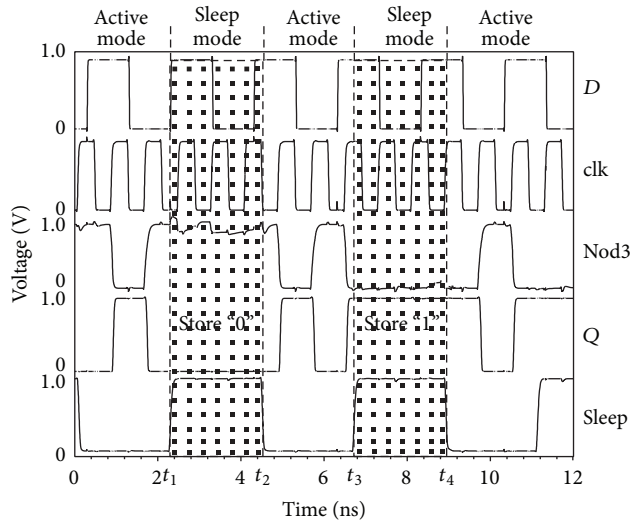

Figure 9: The simulation waveform of the ADR-FF.

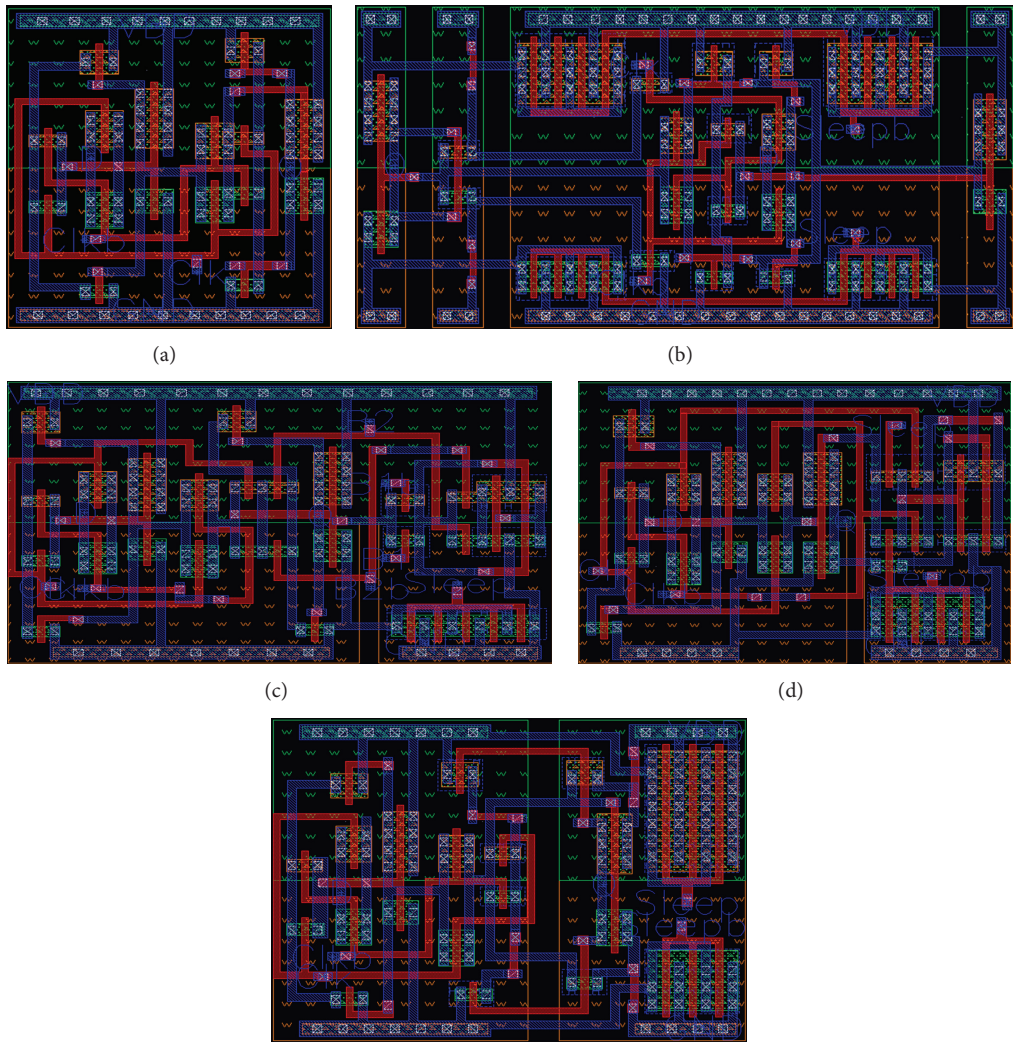

Figure 10: The layouts of different flip-flops: (a) ST-TG-FF, (b) Mutoh-FF, (c) Balloon-FF, (d) Memory-TG-FF, and (e) ADR-FF.

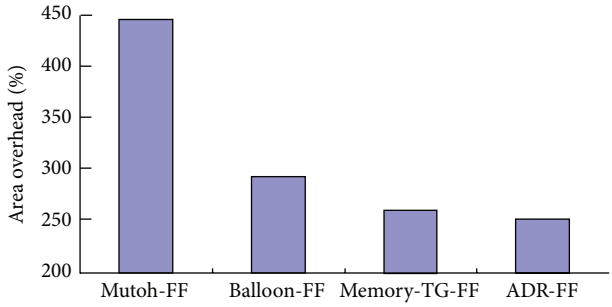

Figure 11: The area overhead of different flip-flops as compared to ST-TG-FF.

Table 3: Total active power, clock power, and leakage power dissipation of different flip-flops.

Flip-flops	Active power (nW)	Clock power (nW)	Leakage power (nW)	
			25°C	110°C
Mutoh-FF	1078.82	50.02	89.75	123.94
Balloon-FF	1011.60	49.17	46.09	78.73
Memory-TG-FF	1125.72	46.51	45.55	84.86
ADR-FF	1067.34	46.43	43.63	89.42

with the previously published data retention flip-flops, it has a lower control circuitry overhead. Moreover, when the flip-flop enters the sleep mode, the output node is not floating, and it keeps the state before sleep mode. And when the flip-flop enters the active mode, the stored state will recover to output node first.

4.2. Power Consumption and Performance of Different Flip-Flops. The active power, clock power, leakage power consumption, and delay of the proposed ADR-FF are evaluated and compared with previous data retention flip-flops in this section. The postlayout simulations are done using HSPICE with the power supply 1.0 V. For fair comparison, all the flip-flops have the same clock and input data. The frequency of the clock and data is 1 GHz and 500 MHz, respectively. The sleep mode leakage power consumption of flip-flops is measured at two different temperature 25°C and 110°C. Power dissipation of the circuits is listed in Table 3.

From Table 3, we can see that the ADR-FF consumes the almost equal active power among the flip-flop circuits with different techniques. The active power consumption of ADR-FF increases 5.51% compared with Balloon-FF. The ADR-FF decreases the active power consumption by 1.06% and 5.19% compared with Mutoh-FF and Memory-TG-FF, respectively. The ADR-FF consumes smaller active power due to the more compact data retention cell. And the transistors number of the ADR-FF is also smaller than other data retention flip-flops.

The ADR-FF, Balloon-FF and Memory-TG-FF have almost equal clock power dissipation because clock signal of these flip-flops has about the same capacitive load due to the similar master-slave structure. The Mutoh-FF consumes the highest clock power among the data retention flip-flops.

Compare with the Mutoh-FF, the leakage power of the ADR-FF decreases 51.39% and 27.85%, at 25°C and 110°C, respectively. The ADR-FF decreases the leakage power 5.34% and 4.22% compared with Balloon-FF and Memory-TG-FF at 25°C. However, at 110°C, the leakage power increases 13.58% and 5.37%, respectively.

To evaluating the delay overhead of the different data retention techniques, the same design parameters are adapted in the master and salve stages of the different flip-flops as shown in Figures 1, 2, 4, 6, and 8. The postlayout simulations of the flip-flops are carried out using HSPICE.

According to the simulation results listed in Table 4, the delay time of Mutoh-FF, Balloon-FF, Memory-TG-FF, and ADR-FF increases 111.83%, 22.06%, 37.54%, and 56.80% as compared to ST-TG-FF, respectively. The delay time of the ADR-FF decreases by 25.98% compared with Mutoh-FF. However, compare with Balloon-FF and Memory-TG-FF, the delay of the ADR-FF increases 27.90% and 14.00%, respectively. The high-V_{th} inverter I5 of the DRC attached to the slave stage of the ADR-FF introduces extra parasitic capacitor in the critical path of the ADR-FF. The parasitic capacitance at the node 3 and output node Q increase the delay time of the ADR-FF.

The state transition times of different data retention flip-flops are simulated. The simulation results are listed in Table 5. The state transition time includes sleep-in time and sleep-out time, which is defined as the entering and leaving sleep mode time, respectively.

As is shown in Table 5, the state transition time of ADR-FF is smaller than other traditional data retention flip-flops. The average state transition time of ADR-FF reduces 55.98%, 51.35%, and 21.07% as compared with Mutoh-FF, Balloon-FF, and Memory-TG-FF, respectively. The lightest overhead of sleep signal and the compact control complexity of ADR-FF cause the minimum state transition time among the traditional data retention flip-flops.

4.3. Area Comparison of Different Flip-Flops. The layouts of flip-flops are optimized many times, and the best layouts are shown in Figure 10. The layout areas are listed in Table 6. The area overheads of the different flip-flops as compared to ST-TG-FF are shown in Figure 11.

Figure 11 shows that area of ADR-FF is the most small during the previous proposed data retention flip-flops. The ADR-FF reduces the area by 35.48% compared with Mutoh-FF and decreases by 10.22% and 4.75% compared with Balloon-FF and Memory-TG-FF, respectively.

5. Conclusions

A new low leakage autonomous data retention flip-flop is presented in this paper. Two sleep transistors are employed to disconnect the low-V_{th} master and slave stages from power supply and ground rails in sleep mode. A small high-V_{th} inverter combined with the slave latch constitutes the data retention cell. Due to the improved circuit structure, no

Table 4: Delay of different flip-flops.

Flip-flops	clk-to-Q (ps)		Setup time (ps)		Delay (ps)
	Tc-q(l-h)	Tc-q(h-l)	Tsu(l-h)	Tsu(h-l)	
ST-TG-FF	52.74	49.61	6.14	12.08	61.69
Mutoh-FF	117.32	68.60	13.36	26.39	130.68
Balloon-FF	69.15	61.66	6.48	11.59	75.63
Memory-TG-FF	76.78	70.66	6.25	14.19	84.85
ADR-FF	87.41	82.86	9.13	13.87	96.73

Table 5: The state transition time of different data retention flip-flops.

Flip-flops	Mutoh-FF	Balloon-FF	Memory-TG-FF	ADR-FF
State transition time				
Sleep-in (ps)	129.00	110.82	68.23	52.14
Sleep-out (ps)	114.91	109.90	67.81	55.03
Average state transition time (ps)	121.96	110.36	68.02	53.69

Table 6: Area of different flip-flops.

Flip-flops	ST-TG-FF	Mutoh-FF	Balloon-FF	Memory-TG-FF	ADR-FF
Area (um^2)	2.63	14.29	10.27	9.68	9.22

extra signals and operations are required for data storing and recovering to and from data retention cell. Hence the control complexity of the proposed the ADR-FF is significantly reduced as compared to the previous data retention flip-flops. Moreover, the problem of the output node floating in the sleep mode of the previous data retention flip-flops is eliminated because of the always powered data retention cell.

The postlayout simulation results show that the ADR-FF consumes the almost equal active power among the flip-flop circuits with different techniques. The leakage power dissipation of the ADR-FF decreases 51.39% and 27.85% compared with Mutoh-FF at 25°C and 110°C, respectively. At 25°C, the ADR-FF reduces the leakage power by 5.34% and 4.22% compared with Balloon-FF and Memory-TG-FF. The average state transition time of ADR-FF decreases 55.98%, 51.35%, and 21.07% as compared with Mutoh-FF, Balloon-FF, and Memory-TG-FF, respectively. Moreover, the layout area of the ADR-FF is reduced up to 35.48%, 10.22%, and 4.75% compared with Mutoh-FF, Balloon-FF, and Memory-TG-FF, respectively.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

Acknowledgments

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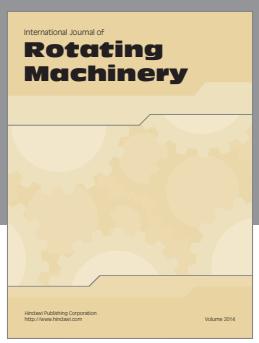

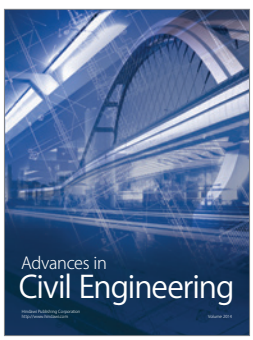

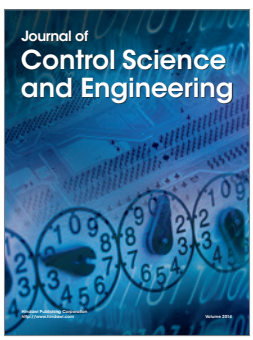

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