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Research Article

Two New Families of Floating FDNR Circuits

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Two new configurations for realizing ideal floating frequency-dependent negative resistor elements (FDNR) are introduced. The proposed circuits are symmetrical and are realizable by four CCII or ICCII or a combination of both. Each configuration is realizable by eight different circuits. Simulation results are included to support the theory.

1. Introduction

The frequency-dependent negative resistor (FDNR) element was introduced by Bruton [1] and used in the realization of ladder filters. Using the operational amplifier (Op Amp) as the active element, Antoniou introduced several realizations of the current generalized impedance converter (CGIC) which was used in active network synthesis of voltage transfer functions [2]. The GIC can also be used in the realization of grounded and floating inductors or FDNR elements [3].

The current conveyor (CCII) [4] was used in realizing grounded and floating inductors and FDNR elements. The first realization in the literature for realizing an ideal grounded FDNR was reported in [5] and it employs a single CCII+, two capacitors, and four resistors, and it requires conditions on the magnitudes of the passive elements. The minimum number of passive elements to realize an ideal FDNR is two capacitors and one resistor. The circuits shown in Figure 1 fulfill this minimum passive element condition and realize an ideal floating FDNR and each circuit uses two; CCII+ and one CCII− [6, 7]. Two alternative realizations of the ideal FDNR using minimum passive components were introduced in [8] using two CCII and a buffer. The circuit shown in Figure 2(a) uses a CCII to realize the buffer and has the disadvantage that the capacitor C_1 is in series with R_{X3} and the capacitor C_2 is in series with R_{X2} thus limits the frequency of operation of the circuit [9]. The circuit shown in Figure 2(b) was also introduced in [8] and avoids the direct connection of a capacitor to the X terminal of a CCII. Four more ideal floating FDNR circuits using two CCII and a negative impedance converter (NIC) were proposed in [10], two of them have capacitors connected to port X of the CCII. The circuit shown in Figure 3(a) uses two; CCII+ and one CCII− and realizes ideal floating inductor by using Y_1 and Y_3 as resistors and Y_2 as a capacitor [11]. The circuit can also be used to realize an ideal FDNR by taking Y_1 as C_1, Y_2 as R, and Y_3 as C_2. In this case, however, the parasitic resistances R_{X1} and R_{X2} will act in series with C_2 and C_1, respectively, and degrades the circuit operation at high frequencies [9]. An alternative floating inductor circuit using three CCII and one CCI was given in [12], although the circuit can be modified using RC:CR transformation [3] to realize an ideal floating FDNR, the two capacitors will be connected to the X terminals of two CCII which will affect the circuit operation as in the previous circuit.

A two CCII− realization of a floating FDNR was introduced in [13] and is shown in Figure 3(b). This realization uses two capacitors and three resistors that is, two resistors more than the minimum required number. The floating admittance realized is given by

$$Y = \frac{s^2 C_1 C_2 R_1 R_2}{R_3}. \tag{1}$$

Three more similar circuits were given in [14]; two of them are shown in Figures 3(c) and 3(d) and each realizes a floating FDNR whose admittance is given by (1).

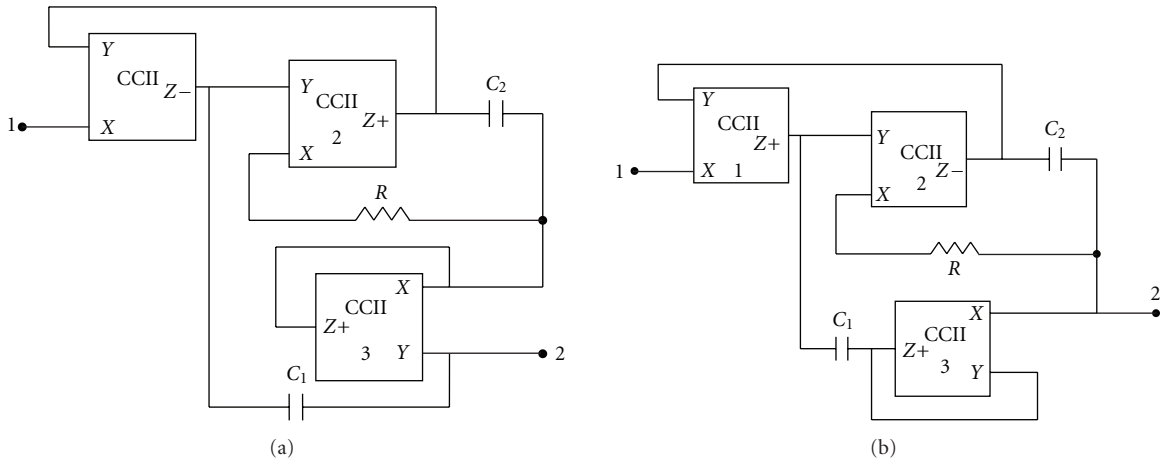

Figure 1: (a) Floating FDNR circuit proposed in [6]. (b) Floating FDNR circuit proposed in [7].

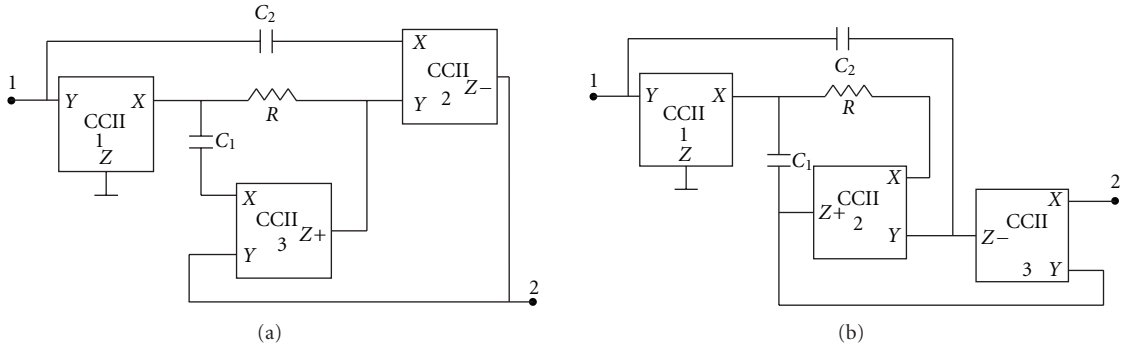

Figure 2: (a) Floating FDNR circuit proposed in [8]. (b) Another floating FDNR circuit proposed in [8].

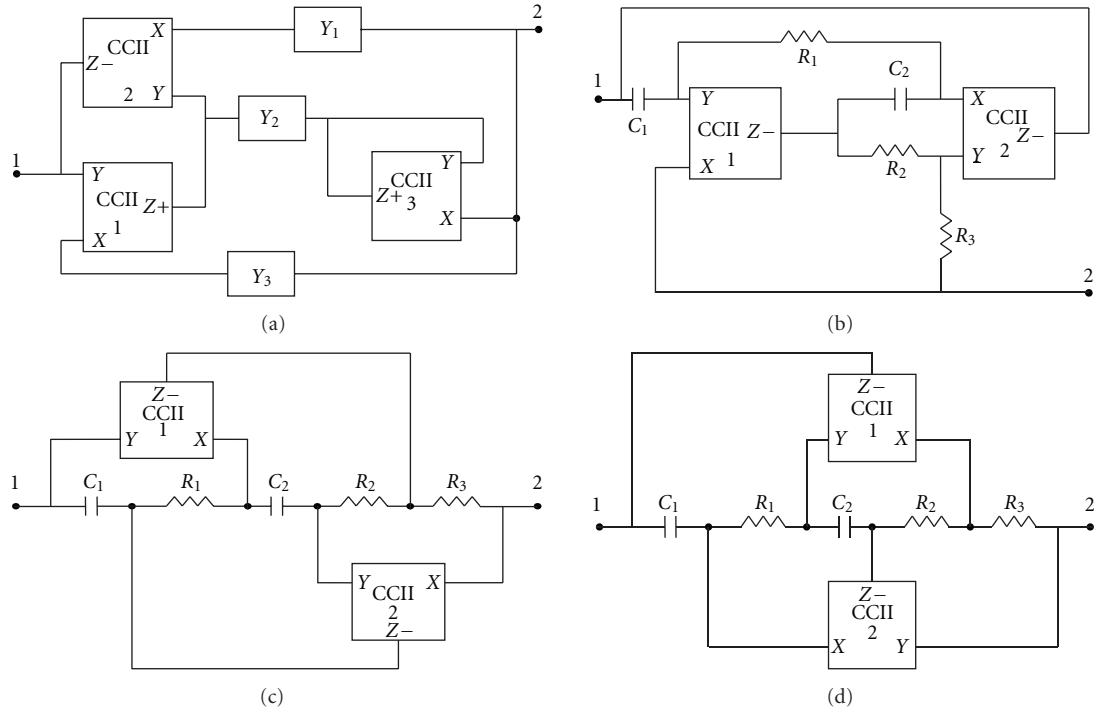

Figure 3: (a) Floating inductor circuit proposed in [11]. (b) Floating FDNR circuit proposed in [13]. (c) Floating FDNR circuit proposed in [14]. (d) Floating FDNR circuit proposed in [14].

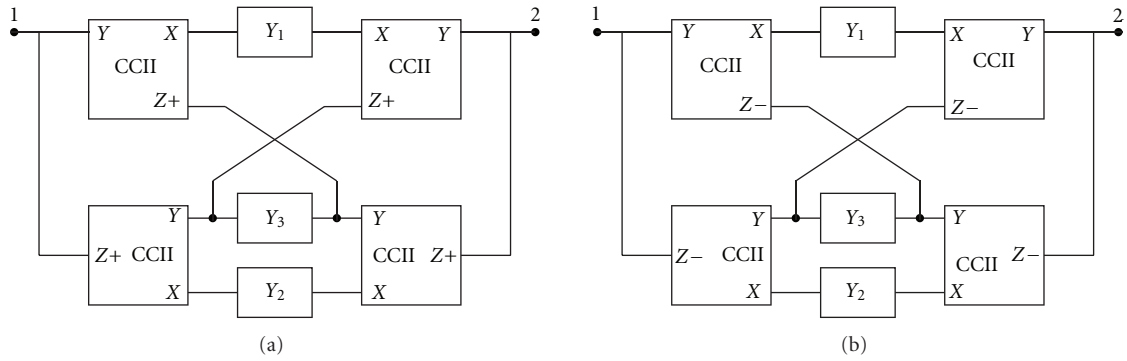

Figure 4: (a) Floating circuit 1 suitable for L realization [15]. (b) Floating circuit 2 suitable for L realization [15, 16].

The circuit shown in Figure 4(a) using four CCII+ realizing ideal floating inductor was introduced in [15]. The circuit is symmetrical and can also employ four CCII− as demonstrated in [16, 17]. Recently the circuit shown in Figure 4(a) is generated using nodal admittance matrix expansion [18] which can also lead to the generation of the circuit shown in Figure 4(b).

Due to the connection of the two capacitors in series with the parasitic resistances R_X of the four CCII, the circuits shown in Figure 4 are not suitable for realizing floating FDNR.

In this paper, two new generalized circuit topologies suitable for floating FDNR realizations are introduced. The first proposed circuit is generated from the circuits of Figure 4 by interchanging ports X and Y of the four CCII and then generalizing the circuit to employ CCII or inverting CCII [19] or a combination of both.

Other realizations for the floating FDNR using nullor [20] operational mirror amplifier [21, 22] and current feedback operational amplifier [23] are available in the literature.

2. Proposed FDNR Configurations

2.1. Generalized Conveyor. The building block that is used in this section is the generalized conveyor (GC) defined by the following matrix equation:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ A & 0 & 0 \\ 0 & K & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}. \tag{2}$$

The parameter A determines the type of the conveyor; a CCII is realized if $A = 1$ and ICCII is obtained if $A = -1$.

The parameter K determines the conveyor Z polarity; for $Z+$ the parameter $K = 1$ and for $Z-$ the parameter $K = -1$.

The GC includes four different types; the CCII− and the ICCII− are floating whereas the CCII+ and ICCII+ are not floating. The CCII+ and ICCII+ although nonfloating can also be used in realizing floating circuits provided they are used in pairs as will be demonstrated in the next section.

2.2. The First New Configuration. Figure 5(a) represents the first proposed generalized floating FDNR circuit. For floating operation, GC1 and GC2 must be identical and GC3 and GC4 must also be identical. It can be shown that the transmission matrix for the circuit of Figure 5(a) is given by

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 1 & \dfrac{A_1K_1A_3K_3}{s^2C_1C_2R} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}. \tag{3}$$

A necessary coefficient condition for realizing a floating FDNR is that

$$A_1K_1A_3K_3 = 1. \tag{4}$$

In this case, the transmission matrix given by (3) realizes a floating admittance given by

$$Y = s^2C_1C_2R. \tag{5}$$

The coefficient condition given by (4) is satisfied by eight alternative realizations as given in Table 1.

2.3. The Second New Configuration. Figure 5(b) represents the second proposed generalized floating FDNR circuit. For floating operation, GC1 and GC2 must be identical and GC3 and GC4 must also be identical. It can be shown that the transmission matrix for the circuit of Figure 5(b) is given by

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 1 & -\dfrac{A_1K_1A_3K_3}{s^2C_1C_2R} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}. \tag{6}$$

A necessary coefficient condition for realizing a floating FDNR is that

$$A_1K_1A_3K_3 = -1. \tag{7}$$

In this case, the transmission matrix given by (6) realizes a floating admittance given by (5). The coefficient condition given by (7) is satisfied by eight alternative realizations as given in Table 2.

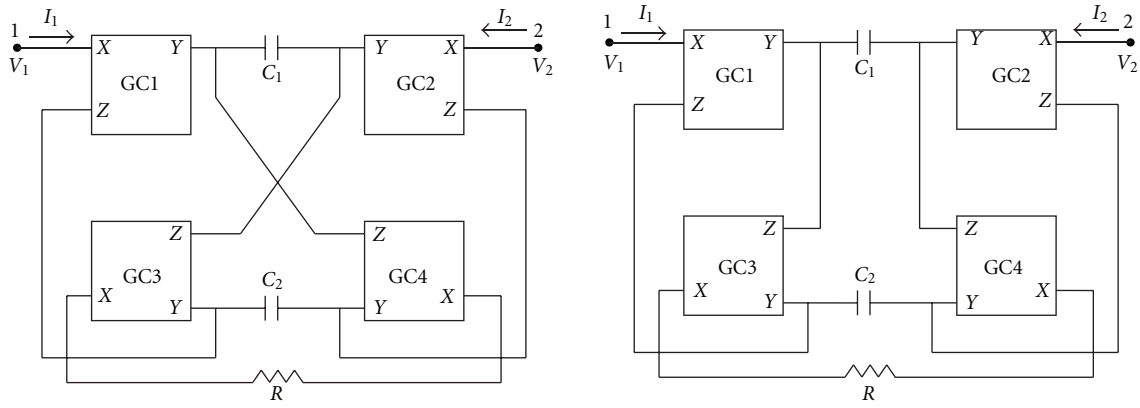

Figure 5: (a) New floating circuit 1 suitable for FDNR realization. (b) New floating circuit 2 suitable for FDNR realization.

Table 1: Eight alternative conveyor circuits based on Figure 5(a).

Circuit	A_1, A_2	K_1, K_2	A_3, A_4	K_3, K_4	GC_1, GC_2	GC_3, GC_4
1	+	+	+	+	CCII+	CCII+
2	+	−	+	−	CCII−	CCII−
3	−	−	+	+	ICCII−	CCII+
4	+	+	−	−	CCII+	ICCII−
5	−	+	−	+	ICCII+	ICCII+
6	−	+	+	−	ICCII+	CCII−
7	+	−	−	+	CCII−	ICCII+
8	−	−	−	−	ICCII−	ICCII−

Table 2: Eight alternative conveyor circuits based on Figure 5(b).

Circuit	A_1, A_2	K_1, K_2	A_3, A_4	K_3, K_4	GC_1, GC_2	GC_3, GC_4
1	+	−	+	+	CCII−	CCII+
2	+	+	+	−	CCII+	CCII−
3	−	+	+	+	ICCII+	CCII+
4	+	+	−	+	CCII+	ICCII+
5	+	−	−	−	CCII−	ICCII−
6	−	+	−	−	ICCII+	ICCII−
7	−	−	+	−	ICCII−	CCII−
8	−	−	−	+	ICCII−	ICCII+

3. Simulation Results

The active building block used in the simulations is the differential voltage current conveyor (DVCC) shown in Figure 6 [24]; the MOS transistor aspect ratios are given in Table 3 based on the 0.5 μm CMOS model from MOSIS. The supply voltages used are ± 1.5 V, $V_{B1} = -0.52$ V, and $V_{B2} = 0.33$ V. The Spice simulation results for two of the new FDNR circuits numbers 1 and 8 in Table 2 are shown in Figure 7.

Table 3: Dimensions of the MOS Transistors of Figure 6.

MOS Transistors	$W(\mu m)/L(\mu m)$
M_1, M_2, M_3, and M_4	2.5/1
M_5 and M_6	8/1
M_{12}, M_{13}, M_{14}, M_{15}, and M_{16}	20/2.5
M_7 and M_8	10/1
M_9, M_{10}, M_{11}, M_{17}, and M_{18}	40/2

The FDNR circuit is designed by taking $C_1 = C_2 = 10$ pF and $R = 1$ kΩ. The circuit is excited at port 1 by a current source of 1 mA, and port 2 is grounded. The frequency response of V_1 is shown in Figure 7(a) and the power dissipation is 3.79746 mW. The simulation are repeated by exciting port 2 by the current source and simulating V_2, an identical frequency response is obtained, which proves that the circuit is symmetrical as expected.

The simulation results for the circuit number 8 specified in Table 2 is shown in Figure 7(b) and the power dissipation is 4.00417 mW.

4. Discussion of Nonidealities

The main objective of the paper is to present new symmetrical circuits realizing floating FDNR circuits using minimum passive elements and avoiding the connection of the two capacitors to the X terminals of the CCII or the ICCII.

It may be useful to discuss the nonidealities in the following subsections.

4.1. Voltage and Current Tracking Errors. There are nonidealities associated with typical CCII and ICCII devices represented in voltage and current tracking errors between the Y and X terminals and the X and Z terminals, respectively. These tracking errors show up as nonunity voltage and current gains between the Y and X terminals and X and Z terminals, respectively. The actual characteristics of

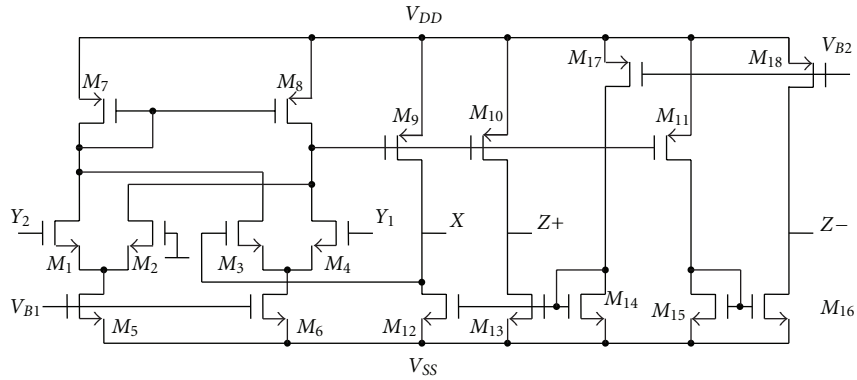

Figure 6: CMOS circuit of the DVCC used in the simulations [24].

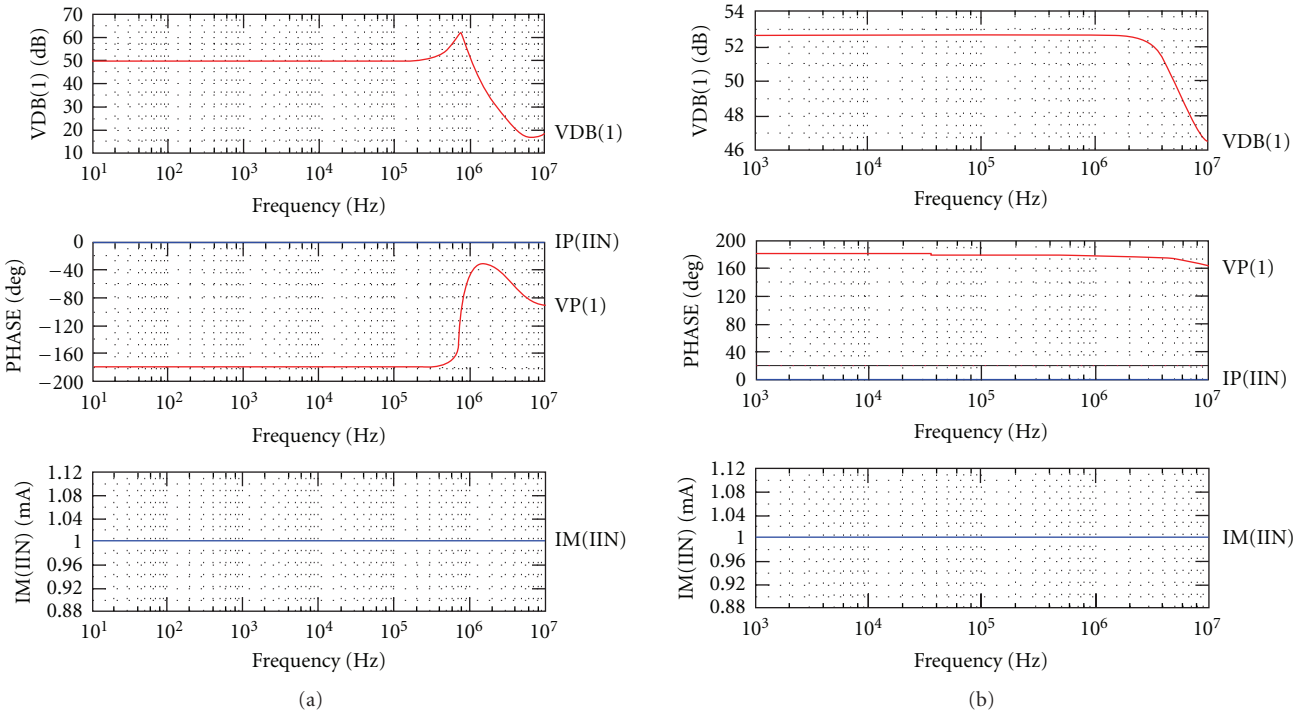

Figure 7: (a) Frequency response of the FDNR realization 1 in Table 2. (b) Frequency response of the FDNR realization 8 in Table 2.

the CCII or the ICCII can be represented by the following matrix equation:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ \pm(1-\alpha) & 0 & 0 \\ 0 & \pm(1-\beta) & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}. \quad (8)$$

The plus sign in the second row applies to CCII and the negative sign applies to ICCII. The plus sign in the third row applies to CCII+ or ICCII+ and the negative sign applies to CCII− or ICCII−, where α and β are the voltage and current tracking errors and are very small compared to unity. The actual values of α and β depend on the actual implementation of the CCII and the ICCII.

Taking these errors into consideration and assuming a symmetrical circuit, GC1 and GC2 are matched and GC3 and GC4 are also matched; the actual value of the magnitude of the FDNR can be obtained as

$$D = \frac{C_1 C_2 R}{(1-\alpha_1)(1-\alpha_3)(1-\beta_1)(1-\beta_3)}. \quad (9)$$

Assume equal alphas and betas, the above equation is simplified to

$$D = C_1 C_2 R(1 + 2\alpha_1 + 2\beta_1). \quad (10)$$

4.2. Effect of Parasitic Elements. According to the CCII or ICCII model, we include the parasitic elements that are mainly represented by the X terminal resistance R_X and the Z terminal capacitance C_Z.

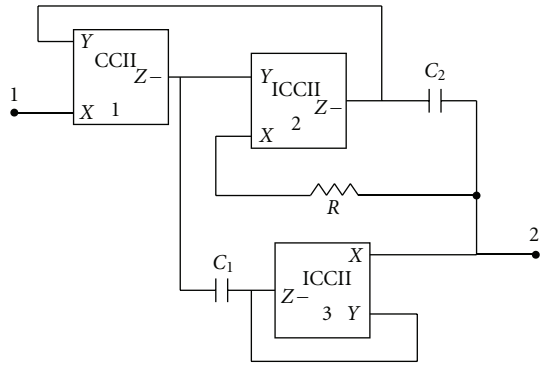

Figure 8: Floating FDNR realization using one CCII− and two ICCII−.

The effect of the parasitic resistances R_{X3} and R_{X4} acting in series with the resistor R is to increase the magnitude of the FDNR value to be

$$D = C_1C_2(R + R_{X3} + R_{X4}). \tag{11}$$

This effect can be internally compensated by reducing the value of the resistor R by $(R_{X3} + R_{X4})$.

The effect of the parasitic resistances R_{X1} and R_{X2} is to add a series resistance to the realizable FDNR equal to $R_{X1} + R_{X2}$. This cannot be internally compensated; however, external compensation is possible using an active negative resistor of same value in series with the FDNR circuit. The two capacitors provided by the Z terminals of the GC1and GC2 will appear at the two nodes of the capacitor C_2 and their effect can be minimized by taking large value of C_2.

Similarly, the two capacitors provided by the Z terminals of the GC3 and GC4 will appear at the two nodes of the capacitor C_1 and their effect can be minimized by taking large value of C_1.

5. Conclusions

A review of early published floating FDNR circuits using CCII is given. A new floating FDNR circuit using a CCII− and two ICCII− is derived from the well-known circuit of Figure 1(b) and is shown in Figure 8.

Two new configurations for realizing ideal floating FDNR are introduced. The proposed circuits are symmetrical and are realizable by four CCII or ICCII or combination of both. Each configuration is realizable by eight different circuits. The main advantage of the proposed circuits is avoiding the capacitors to be connected to the X terminals of the CCII or ICCII. Simulation results are included to support the theory.

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