Hindawi
Active and Passive Electronic Components
Volume 2019, Article ID 8425198, 7 pages
https://doi.org/10.1155/2019/8425198

Research Article

Improving Linearity and Robustness of RF LDMOS by Mitigating Quasi-Saturation Effect

Haifeng Mo,[1,2] **Yaohui Zhang**,[1] **and Helun Song**[1]

[1] *Suzhou Institute of Nano-Tech and Nano-Bionics, Chinese Academy of Sciences, China*
[2] *University of Chinese Academy of Sciences, China*

Correspondence should be addressed to Haifeng Mo; hfmo2015@sinano.ac.cn

Received 21 February 2019; Revised 20 June 2019; Accepted 26 June 2019; Published 14 July 2019

Academic Editor: Gerard Ghibaudo

This paper discusses linearity and robustness together for the first time, disclosing a way to improve them. It reveals that the nonlinear transconductance with device working at quasi-saturation region is significant factor of device linearity. The peak electric field is the root cause of electron velocity saturation. The high electric field at the drift region near the drain will cause more electron-hole pairs generated to trigger the parasitic NPN transistor turn-on, which may cause failure of device. Devices with different drift region doping are simulated with TCAD and measured. With LDD4 doping, the peak electric field in the drift region is reduced; the linear region of the transconductance is broadened. The adjacent channel power ratio is decreased by 2 dBc; 12% more power can be discharged before the NPN transistor turn-on, indicating a better linearity and robustness.

1. Introduction

Linearity and robustness are very important in power amplifier of base station communication. For LDMOS power devices, the relationship between output and input signal is close to the square relationship in saturation region, which is very prone to spectrum leakage and intermodulation distortion. In addition, the capacitance exhibits a nonlinear relationship with the voltage, which easily generates phase distortion. In communication applications, devices always work with back-off to meet linearity requirements, which sacrifice efficiency, especially for asymmetric Doherty amplifiers [1]. The adjacent channel power ratio (ACPR) is an indicator to measure the linearity of power amplifier; it is defined as the ratio of power density of the offset channel to the power density of the main channel.

The research of linearity of RF LDMOS focuses on the linearity of capacitance and transconductance. Paper [2] studied the effects of input capacitance on intermodulation distortion (IMD) and AM-PM distortion under the two-tone signal input of class A power amplifier from the simulation point of view. Paper [3] revealed that the low-frequency IMD related to the nonlinearity of transconductance, while the high-frequency IMD related to the nonlinearity of transconductance and capacitor. In paper [4], multiple LDMOS were combined in parallel; each was biased at different voltages; then IMD was reduced by combination of different sweet spots. Paper [5] reduced the size of the drain contact to increase the saturation current.

Robustness is the ability of LDMOS to withstand the power from output mismatched or the power from electrostatic discharge. Robustness of LDMOS correlated with the inherently presented parasitic bipolar NPN transistor [6], and more body doping was suggested to suppress the turn-on of NPN transistor. The device could fail because of formation of early filament [7, 8]; deep implantation drain contact [9] and ESD implantation at drain side [10] were suggested to address the formation of early filament issue.

This paper discusses the linearity and robustness together for the first time. Electric field distribution and transconductance of devices with different drift region doping are simulated with TCAD. The peak electric field of drift region can be reduced by adjusting the doping of drift region, resulting in better linearity and robustness, verified by silicon data. Section 2 of this thesis analyzes the relationship between transconductance and linearity, analyzes the relationship

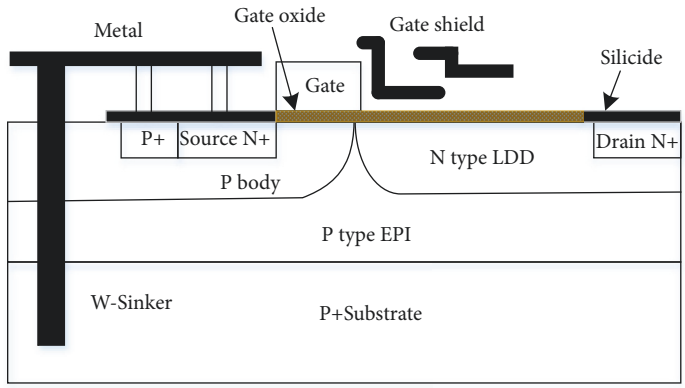


Figure 1: Structure of RF LDMOS.

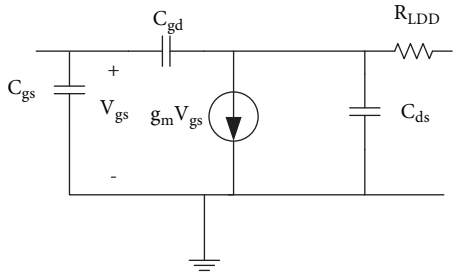


Figure 2: Equivalent circuit of RF LDMOS.

between quasi-saturation effect and electric field distribution in the drift region, and proposes a scheme to improve the linearity of transconductance and robustness. The test results and discussion are shown in Section 3. And Section 4 concludes this paper.

2. Methods and TCAD Simulation

Figure 1 is a schematic diagram of the structure of LDMOS device; Figure 2 is the small-signal equivalent circuit of the device, where R_{LDD} is the equivalent resistance of the drift region, and g_m is the transconductance of the device. According to the Miller effect, the transconductance of the device is represented by G_m as shown in formula (1). The linearity can be improved in two ways, one is to improve the linearity of the transconductance, and the other is to reduce the Miller capacitance C_{gd} and the output capacitance C_{ds}. This paper optimizes the linearity of transconductance by mitigating the quasi-saturation effect.

$$G_m = \frac{g_m - j\omega C_{gd}}{1 + j\omega \left(C_{gd} + C_{ds}\right) R_{LDD}} \quad (1)$$

The space charge modulation effect is the cause of current saturation [11, 12]; on one hand, it decreases the mobility of electrons, and on the other hand, it narrows the depletion layer between the channel edge and the drift region. The reduction of mobility is due to the increase of electron density injected into the drift region and the peak electric field near the drain. The higher the peak electric field, the easier the carrier mobility saturated and thus the earlier the current saturation. Correspondingly, there are two methods to mitigate the saturation effect. One is to increase the background concentration, but the breakdown voltage and the reliability of the hot carrier injection will be sacrificed. The second is to reduce the drift region length, which will sacrifice the breakdown voltage and robustness. To get a good trade-off between linearity, efficiency, breakdown voltage, HCI reliability, and robustness, the peak electric field in the drift region has to be flatten. The electric field and transconductance of different drift region structure are simulated with TCAD.

Figure 3 is a diagram of the doping structure of the drift region. The length of the drift region is 2.8 um. LDD1 indicates the first N-type implantation in the entire drift region; the energy is 100KEV. LDD2 is the second N-type implantation with the energy of 200KEV; the distance to the gate edge is 0.8um. LDD3 is the third N-type implantation with the energy of 200KEV; the distance to the gate edge is 1.4um. LDD4 is the fourth N-type implantation with the energy of 200KEV; the distance to the gate edge is 2.2μm. The dosage of each implantation is shown as L1D, L2D, L3D, and L4D in Table 1. This step doping profile structure can increase the FOM value of breakdown voltage and on-resistance, especially in super junction structures [13].

Table 1 lists the doping condition and DC simulation results of device with different drift region doping. Drain saturation current increase as the total doping of drift region. As illustrated in Figure 4, transconductance and saturated drain voltage increase as doping of drift region, the saturation point shifted to a larger drain current, and the linear region of transconductance is broadened, indicating better linearity. Transconductance of device with LDD4 doping increases significantly, while only little change was found when doped with LDD3 after LDD4. It is because the electric field of the drift region is optimized with LDD4 doping; more doping would not cause significant change of the electric field and thus the transconductance. As illustrated in Figure 5, similar transconductance can be obtained, by increasing the width of LDD4 or by increasing the dose of LDD4.

Table 1: DC simulation results and doping condition of different devices.

Condition	LDD4 to Poly (um)	LDD1 Dose (cm^{-2})	LDD2 Dose (cm^{-2})	LDD3 Dose (cm^{-2})	LDD4 Dose (cm^{-2})	Breakdown voltage (V)	Threshold voltage (V)	R_{dson} (ohm∗mm)	I_{dsat} (mA/mm)
A	NA	1.8E+12	8.0E+11	NA	NA	70.15	1.25	13.25	177
B	2.2	1.8E+12	8.0E+11	NA	6.0E+11	70.76	1.26	12.83	179.7
C	2.2	1.8E+12	8.0E+11	NA	1.0E+12	70.55	1.26	12.77	180.3
D	2.2	1.8E+12	8.0E+11	NA	1.4E+12	71.41	1.26	12.52	182.5
E	2.2	1.7E+12	7.0E+11	5.0E+11	1.0E+12	71.52	1.26	12.21	183.2
F	2.2	1.7E+12	7.0E+11	7.0E+11	1.0E+12	70.75	1.26	11.87	185
G	2.2	1.7E+12	8.0E+11	7.0E+11	1.0E+12	70.25	1.26	11.62	189.6
H	2	1.8E+12	8.0E+11	NA	1.0E+12	70.15	1.26	12.62	181.2
I	2.4	1.8E+12	8.0E+11	NA	1.0E+12	70.51	1.26	12.99	178.1

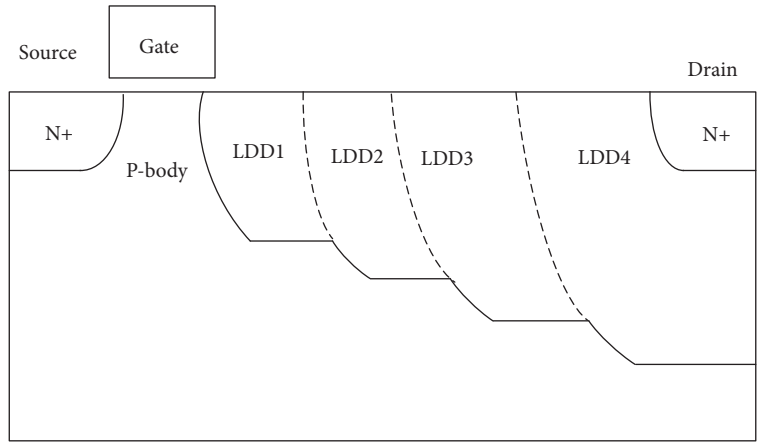


Figure 3: Structure of LDMOS drift region.

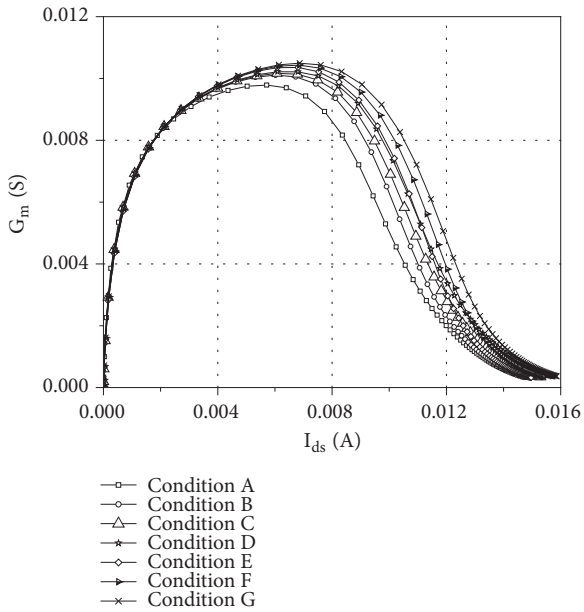


Figure 4: G_m of devices with different doping of drift region.

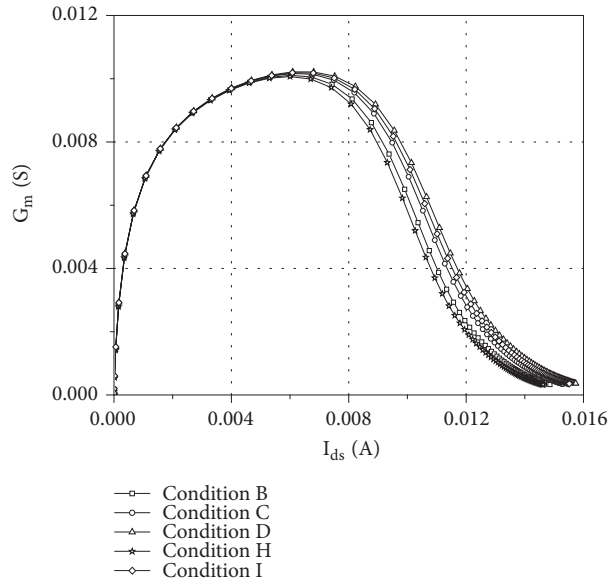
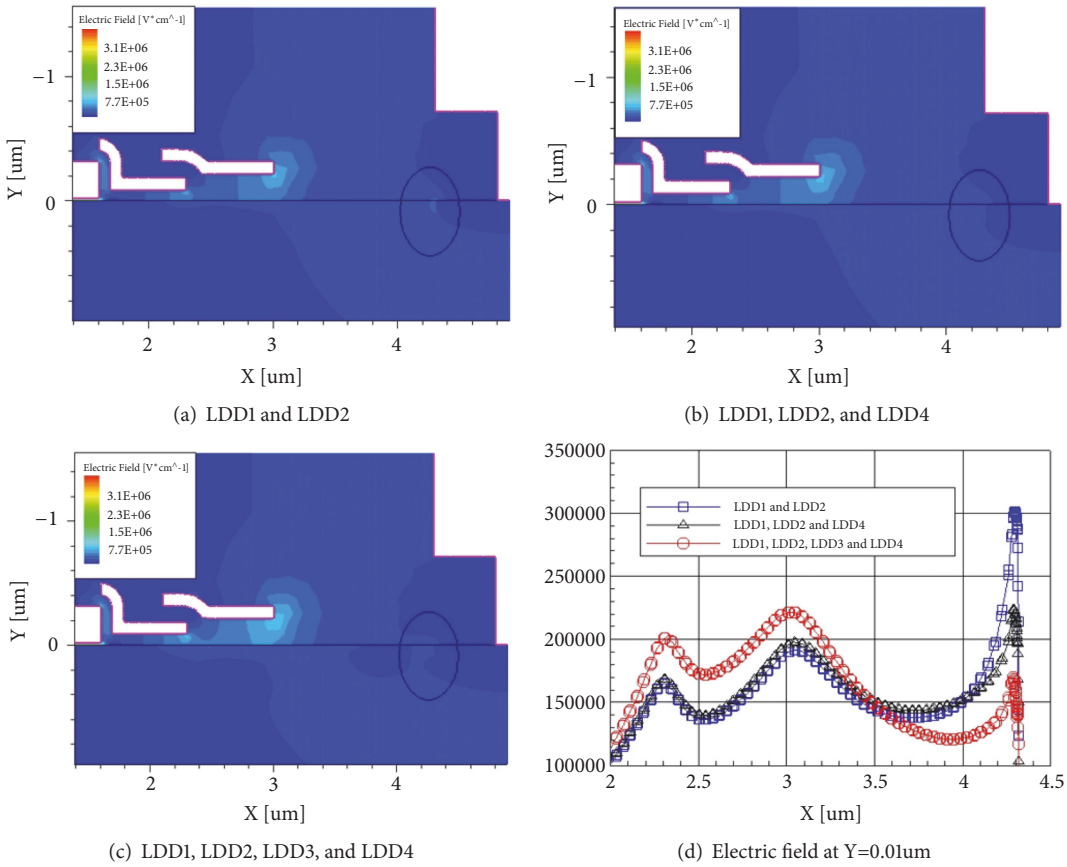


Figure 5: G_m of devices with different length and doping of drift region.

The electric field distribution under quasi-saturation condition is illustrated in Figure 6. The black ellipse box in the figure is the interface of drift region and the drain contact, where the peak electric field located. This peak electric field decreases after LDD4 is implanted and decreases as the number of LDD increases. The graded doping near the drain results in a uniform distribution of the electric field. The peak electric field in the drift region of device with LDD4 doping reduces significantly, resulting in a broadened linear region of transconductance. Increasing the number of LDD's implantation reduces the peak electric field near the drain, making the electric field distribution in the drift region more uniform, reducing the saturation of the carriers, thereby mitigating the quasi-saturation effect of the device.

The electrical equivalent circuit corresponding to the robustness is given in Figure 7. Under output mismatch condition, high power returned to the LDMOS drain, leading to high drain voltage, resulting in strong electric field at the drift region. Then more electron-hole pairs are generated and the hole current may trigger the conduction of NPN transistor, leading to formation of early filament [7, 8], which may cause failure of device. To improve robustness, the electric field at drift region near the drain has to be decreased to restrain the formation of electron-hole pairs. As the analysis in last paragraph, the electric field at the drain can be uniformed with LDD4 doping.

It can be summarized that the doping distribution near the drain became graded distribution after LDD4 doping, which reduced the peak electric field near the drain, and uniformed the electric field in the drift region. Then the kirk effect is relaxed, thus mitigating the quasi-saturation effect, resulting in a more linear transconductance. Device with more uniform distribution electric field near the drain will have fewer electron-hole pairs generated under mismatch and



(a) LDD1 and LDD2

(b) LDD1, LDD2, and LDD4

(c) LDD1, LDD2, LDD3, and LDD4

(d) Electric field at Y=0.01um

Figure 6: Electric field distribution of device with different LDD structure.

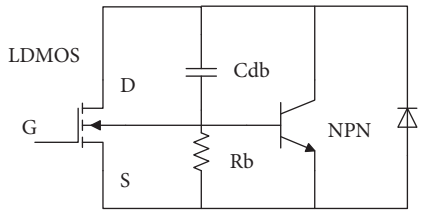


Figure 7: Electric equivalent circuit of LDMOS robustness.

better robustness. The linearity and robustness optimization result will be discussed in next section.

3. Results and Discussion

Referring to the HCI evaluation method of [14], device was stressed at the static biased condition; in this paper, V_{ds} equals 28V and I_{dq} equals 8mA/mm. Then on-resistance and drain current I_{dq} were drawn versus time to evaluate the device lifetime. The on-resistance and static drain current degradation of device of condition G with the maximum saturation current, which may have worse HCI, as well as condition C are given in Figure 8. The growth of on-resistance within lifetime is limited to 10%, which will result in 0.3dB reduction of output power. The on-resistance of condition G increases less than 6% within 20 years, which meets the lifetime requirement of base station application.

The transconductance of test structure on wafer of different devices is given in Figure 9. The transconductance increases as doping of drift region, and the saturation effect is mitigated with LDD4 and LDD3 doping, matching with TCAD simulation. As illustrated in Figure 10, 2dBc better ACPR is obtained with LDD4 doping, but no significant change of ACPR was found in device with LDD3 doping after LDD4. It can also be found in Figure 11 that, to some extent, there is no significant change of ACPR when increasing the doping of LDD3. It can be concluded that the linear region of transconductance is broadened with LDD4 doping, and 2dBc better ACPR is obtained, with very little benefit when additional LDD3 is added after LDD4.

To verify the robustness of the devices with doping engineering, devices of conditions A, C, and G are tested under transmission line pulse (TLP) test, as illustrated in Figure 12 and Table 2. With LDD4 doping, V_{t2}, the drain voltage when the parasitic NPN transistor turns on increases from 78 volts to 87.5 volts, which means 12% more power can be discharged, indicating better robustness. No significant change of robustness was found in device with LDD3 doping after LDD4 doping.

The transconductance measurement matches with TCAD simulation; the ACPR and robustness measurement data match with the TCAD simulation conclusion of electric field

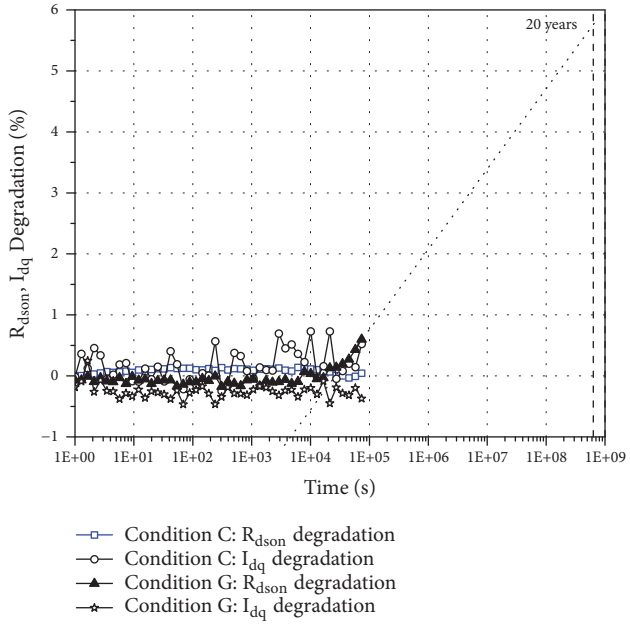


Figure 8: HCI test result of RF LDMOS.

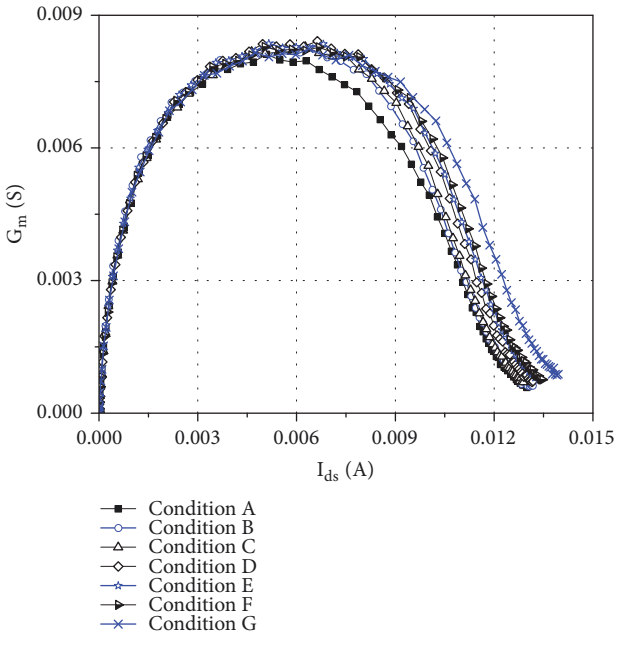


Figure 9: Gm of different device.

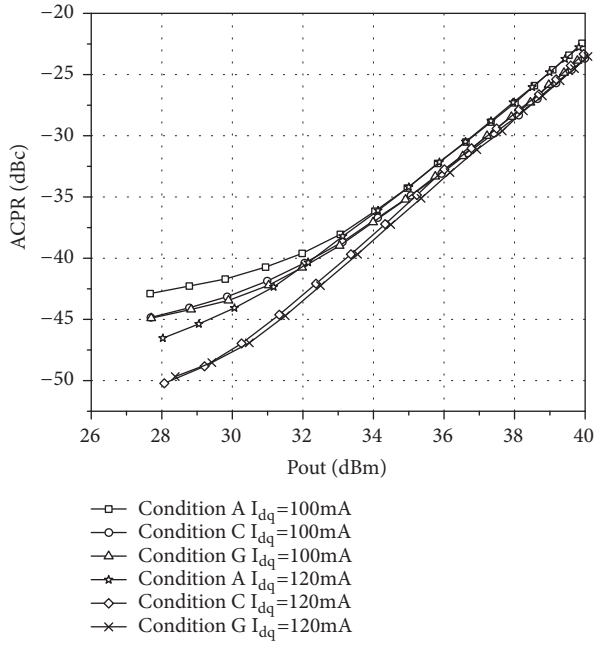


Figure 10: ACPR of conditions A, C, and G.

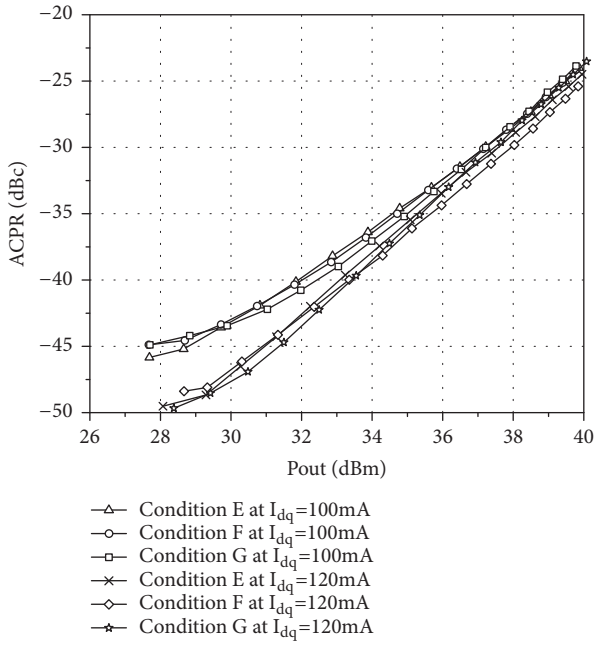


Figure 11: ACPR of device with different LDD3.

distribution. With LDD4 implantation, the concentration gradient between the drain contact and the drift region is reduced, and the gradient decreases as the dosage increases. The peak electric field of the drift region near the drain reduced, resulting in more uniform electric field distribution, which mitigated the saturation effect of the device, making a more linear transconductance, thereby improving the ACPR. Better robustness is also obtained with more uniform distributed electric field.

4. Conclusion

It is revealed and verified by TCAD simulation and measurement data that, by drift region doping engineering, the peak electric field distribution in the drift region is reduced, the quasi-saturation effect of the device is mitigated, the linearity of the transconductance is improved, and the ACPR is improved more than 2 dBc. The reduction of the drain peak electric field is also beneficial to the robustness of the device;

Table 2: Robustness results of different devices.

Condition	V_{t1} (V)	V_{t2} (V)	I_{ds} at V_{t2} (A)
Condition A	69.95	78	0.48
Condition C	69.69	87.5	0.46
Condition G	69.83	87.5	0.47

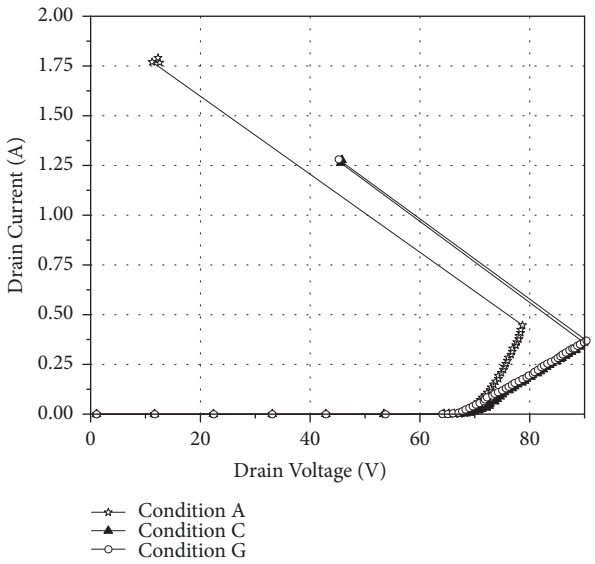


Figure 12: TLP test data of conditions A, C, and G.

12% more power can be discharged before the parasitic NPN transistor turns on.

Data Availability

Experimental results provided in the article were obtained in the System Integration and IC Design Division of Suzhou Institute of Nano-Tech and Nano-Bionics, Chinese Academy of Sciences, in 2018.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

Acknowledgments

This work is supported by the National Key Research and Development Program of China (Grant No. 2016YFE0129400), the Youth Innovation Promotion Association CAS (Grant No. 2016290), the National Defense Basic Scientific Research Program of China (Grant No. JCKY2017210B006), and the Strategic Priority Research Program of the Chinese Academy of Sciences (Grant No. XDC02010800).

References

[1] K. Bathich, H. Portela, and G. Boeck, "A high efficiency Si LDMOS Doherty power amplifier with optimized linearity," in *Proceedings of the SBMO/IEEE MTT-S International Microwave and Optoelectronics Conference, IMOC '09*, pp. 33–36, Brazil, 2009.

[2] O. Bengtsson, L. Vestling, and J. Olsson, "Investigation of the non-linear input capacitance in LDMOS transistors and its contribution to IMD and phase distortion," *Solid-State Electronics*, vol. 52, no. 7, pp. 1024–1031, 2008.

[3] O. Tornblad, C. Ito, F. Rotella, M. Gordon, and R. W. Dutton, "Linearity analysis of RF LDMOS devices utilizing harmonic balance device simulation," in *Proceedings of the International Conference on Simulation of Semiconductor Processes and Devices, SISPAD '05*, pp. 243–246, 2005.

[4] M. van der Heijden, H. de Graaff, L. de Vreede, J. Gajadharsing, and J. Burghartz, "Ultra-linear distributed class-AB LDMOS RF power amplifier for base stations," in *Proceedings of the IEEE MTT-S International Microwave Symposium Digest '01*, vol. 2, pp. 1363–1366, Phoenix, Ariz, USA.

[5] A. Gupta, M. Shrivastava, M. S. Baghini, D. K. Sharma, H. Gossner, and V. R. Rao, "On the improved high-frequency linearity of drain extended mos devices," *IEEE Microwave and Wireless Components Letters*, vol. 26, no. 12, pp. 999–1001, 2016.

[6] S. J. C. H. Theeuwen and J. H. Qureshi, "LDMOS technology for RF power amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 6, pp. 1755–1763, 2012.

[7] M. Shrivastava and H. Gossner, "A review on the esd robustness of drain-extended mos devices," *IEEE Transactions on Device and Materials Reliability*, vol. 12, no. 4, pp. 615–625, 2012.

[8] A. J. Walker, H. Puchner, and S. P. Dhanraj, "High-voltage CMOS ESD and the safe operating area," *IEEE Transactions on Electron Devices*, vol. 56, no. 8, pp. 1753–1760, 2009.

[9] V. Parthasarathy, V. Khemka, R. Zhu, J. Whitfield, A. Bose, and R. Ida, "A double RESURF LDMOS with drain profile engineering for improved ESD robustness," *IEEE Electron Device Letters*, vol. 23, no. 4, pp. 212–214, 2002.

[10] M. Shrivastava, H. Gossner, and C. Russ, "A drain-extended MOS device with spreading filament under ESD stress," *IEEE Electron Device Letters*, vol. 33, no. 9, pp. 1294–1296, 2012.

[11] C.-Y. Chen, O. Tornblad, and R. W. Dutton, "Linearity analysis of lateral channel doping in RF power MOSFETs," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 12, pp. 3389–3394, 2009.

[12] B. S. Kumar and M. Shrivastava, "Part I: on the unification of physics of quasi-saturation in LDMOS devices," *IEEE Transactions on Electron Devices*, vol. 65, no. 1, pp. 191–198, 2018.

[13] Y. Hu, H. Wang, C. Du et al., "A high-voltage (>600 V) N-island LDMOS with step-doped drift region in partial SOI technology," *IEEE Transactions on Electron Devices*, vol. 63, no. 5, pp. 1969–1976, 2016.

[14] D. C. Burdeaux and W. R. Burger, "Intrinsic reliability of RF power LDMOS FETs," in *Proceedings of the 49th International Reliability Physics Symposium, IRPS '11*, pp. 5A.2.1–5A.2.9, 2011.