

Research Article

The I - V Characteristic Prediction of BCD LV pMOSFET Devices Based on an ANFIS-Based Methodology

Shen-Li Chen

Department of Electronic Engineering, National United University, 2 Lien-Da Road, Miaoli City 36003, Taiwan

Correspondence should be addressed to Shen-Li Chen; jackchen@nuu.edu.tw

Received 12 October 2014; Revised 13 February 2015; Accepted 13 February 2015

Academic Editor: Mehmet Onder Efe

Copyright © 2015 Shen-Li Chen. This is an open access article distributed under the Creative Commons Attribution License, which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

Comprehensive and predictive modeling of submicron devices using the traditional TCAD EDA tools of device simulation has become increasingly perplexing due to a lack of reliable models and difficulties in calibrating available device models. This paper proposes a new technique to model BCD submicron pMOSFET devices and to predict device behaviors under different bias conditions and different geometry dimensions by using the adaptive neurofuzzy inference system (ANFIS), which combines fuzzy theory and adaptive neuronetworking. Here, the power of using ANFIS to realize the I - V behaviors is demonstrated in these p-channel MOS transistors. After a systematic evaluation, it can be found that the predicting results of I - V behaviors of complicated submicron pMOSFETs by ANFIS are compared with the actual diagnostic experiment data, and a good agreement has been obtained. Furthermore, the error percentage was no greater than 2.5%. As such, the demonstrated benefits of this new proposed technique include precise prediction and easier implementation.

1. Introduction

The modeling of semiconductor devices most enables the evaluation of device behavior as a function of bias conditions and device geometry parameters. In general, understanding the physical phenomena underlying device behavior leads to the so-called device SPICE model or physical approach [1–6]. Eventually, it creates device model that must cover at least one region of device operation, thus producing the problem of how to model the transitions between them. Therefore, in some cases this approach is not applicable or is too complicated because of a lack of understanding of the device physics.

Actually, for example, for the threshold voltage of a MOSFET, this is a minimum gate voltage which can induce enough carriers to support the current. Together, the threshold voltage and the device dimensions form an important parameter of the BSIM model or the HSpice-based MOSFET circuit model used in the circuit simulation of ULSI design. However, the dimensions of the MOSFETs used in ULSI designs have been continuously reduced in order to achieve

higher device/circuit density. Moreover, it is well known that the threshold voltage V_{th} of a small device will be different from that of a long or wide device due to a combination of the short-channel effect (SCE) [7–9], the narrow-width effect (NWE) [10, 11], the reverse short-channel effect (RSCE) [12, 13], and the reverse narrow-width effect (RNWE) [14, 15]. Meanwhile, the I_d equations of a MOSFET in HSpice are evolved from Level 1 (Shichman-Hodges model) to BSIM3 Level 49 [16–18]. Therefore, the I - V characteristics of MOSFETs cannot be easily expressed by an exact formula in an ULSI circuit simulation. In this context, this work will present a novel method for predicting the characterization of submicrometer pMOSFETs by using a combination of fuzzy theory and a neural network.

In this paper, the ANFIS was developed to solve the problem. This method does not need to assume any fitting parameters, so it can be applied to any physical system. Because fuzzy rules are obtained from human expertise and knowledge, they may sometimes be insufficient and lacking in definition. To improve upon this shortcoming in the fuzzy rules, a neural network algorithm was included in the fuzzy

TABLE 1: All of device geometry dimensions of different DUTs.

Group 1A	L_1	L_2	L_4	L_5	L_6	L_8	L_9	Group 1B	L_3	L_7	L_{10}
L (μm)	0.4	0.45	0.6	0.8	1.0	1.6	2.0	L (μm)	0.5	1.2	3.0
W (μm)	2	2	2	2	2	2	2	W (μm)	2	2	2
Group 2A	W_1	W_2	W_3	W_5	W_6	W_8	W_9	Group 2B	W_4	W_7	W_{10}
L (μm)	0.6	0.6	0.6	0.6	0.6	0.6	0.6	L (μm)	0.6	0.6	0.6
W (μm)	0.5	0.55	0.6	0.8	1.0	1.6	2	W (μm)	0.7	1.2	3

art. This concept included the advantages of both fuzzy control and a neural network system. Using this method, we can add the advantages of a neural network technique, which has learning and calculation ability, into the fuzzy prediction. At the same time, a fuzzy prediction system can also provide a high level of human expertise and fuzzy rules for the neural network. Therefore, a fuzzy system associated with the learning ability of a neural network should lessen the rate of error quite obviously. This architecture is the so-called adaptive neurofuzzy inference system, or ANFIS [19–22]. In some situations a noise may directly affect one's accuracy to perform a task. Initially, a single noise or a measurement outlier may be reduced by the ANFIS network with the learning and training processes. Of course, some front-end filters or denoising methods are needed and also used for good noise cancellations as using the ANFIS [23–27].

The model that was used in this study is based on ANFIS. It was developed to analyze the relation of drain-to-source current (I_d) versus different drain-to-source bias voltages (V_d) and gate-to-source bias voltages (V_g) under different channel lengths (L) and channel widths (W) as in the same fabricated process condition. Using this methodology, the model does not need to fit any physical parameters. The device parameters (the weighting and threshold coefficient) may be evaluated during the learning process according to the measured data.

2. Experimental Details

2.1. Obtain the Experimental Results. In this paper, all of the geometry sizes of the tested devices are listed in Table 1. These testing samples ($L_1 \sim L_{10}$ and $W_1 \sim W_{10}$) were fabricated by the LV process in a $0.4 \mu\text{m}$ BCD technology. The channel width (W) of the group 1 samples was set to be $2 \mu\text{m}$, and the channel length was varied from $0.4 \mu\text{m}$ to $3 \mu\text{m}$ (diagnostic 1B DUTs included). The channel length (L) of the group 2 samples was set to be $0.6 \mu\text{m}$, and the channel width was varied from $0.5 \mu\text{m}$ to $3 \mu\text{m}$ (diagnostic 2B DUTs included). In the first step, the Keithley 236/2361 system was used to measure every DUT to obtain the experimental I - V characteristics of drain current under different drain- and gate-bias voltages. For avoiding some measurement noises, a long integration time (sampling time) was used to get an average data (filter-like) during the device testing by the Keithley 236/2361 system. Furthermore, all of these experimental data can be treated as the training data and the diagnostic prediction values of drain current (I_d).

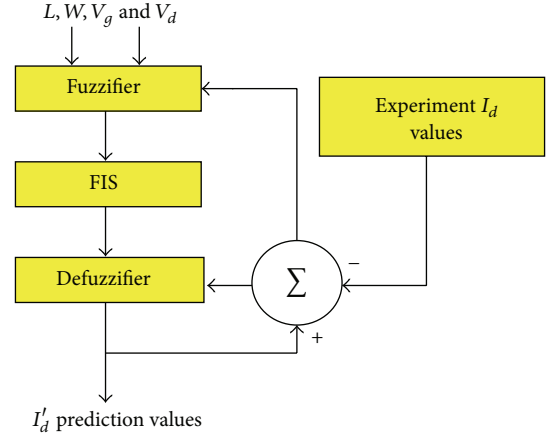


FIGURE 1: ANFIS training flow chart.

2.2. Neurofuzzy Inference System Learning. It is well known that the main problem in MOSFET device modeling is related to the transition from the subthreshold region to the strong-inversion region and the transition from the ohmic region to the saturation region. For the simplest situation, a pMOS transistor can be considered a three-terminal device for which two of the terminals (the source and bulk terminals) are grounded. In this situation, the relation of drain current I_d will be a function of two bias variables (V_d, V_g). However, it is difficult by using an exact and simple formula to express the involvements. Therefore, in this paper, we have used the idea of the adaptive neurofuzzy inference system (ANFIS) to predict the relation of drain current versus four variables (V_g, V_d, L , and W) in pMOSFET devices.

The ANFIS training procedure is described in Figure 1. First, four input parameters were treated as the training data. After training using ANFIS, we were able to obtain the prediction value of drain current I_d' . Figure 2 shows the ANFIS architecture; it includes five layers: the fuzzier layer, product layer, normalize layer, trigger layer, and sum layer.

3. Results and Discussion

In this study, the measured results of samples $L_3, L_7, L_{10}, W_4, W_7$, and W_{10} were treated as the diagnostic data. Furthermore, the measured results of other samples were taken as the preliminary and training data. After ANFIS training, we were able to obtain the I_d prediction values, and the error

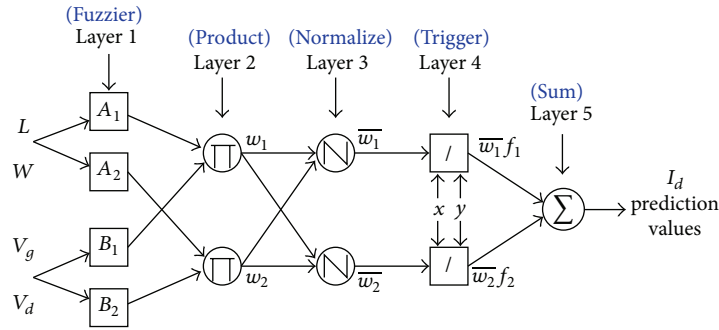


FIGURE 2: Predicting flow chart of I_d values in the ANFIS.

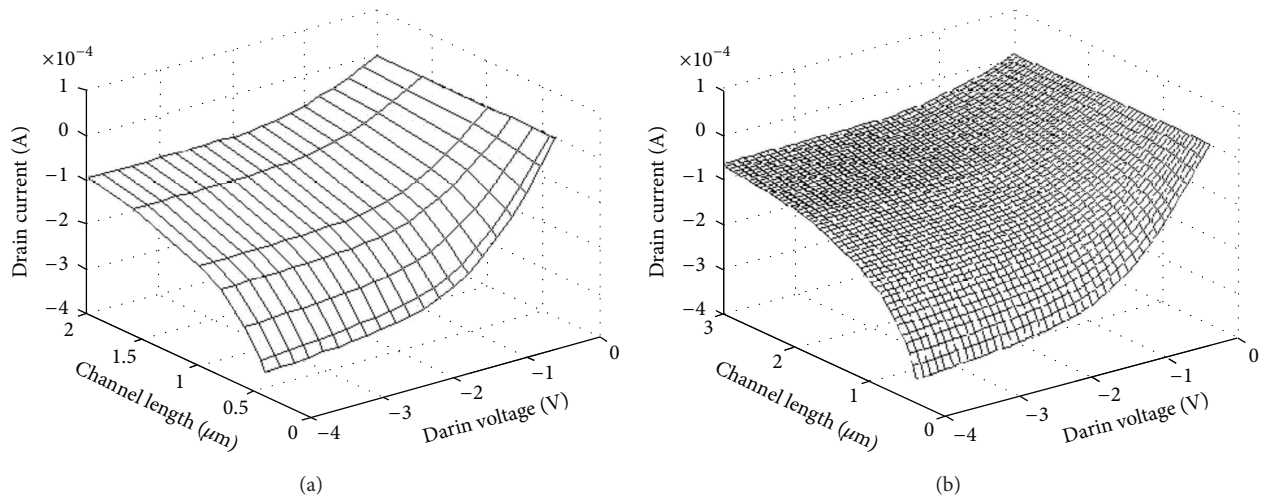


FIGURE 3: The 3D-like I_d (a) measurement data surface and (b) prediction data surface versus L and V_d of the group 1A samples (as $V_g = -3$ V).

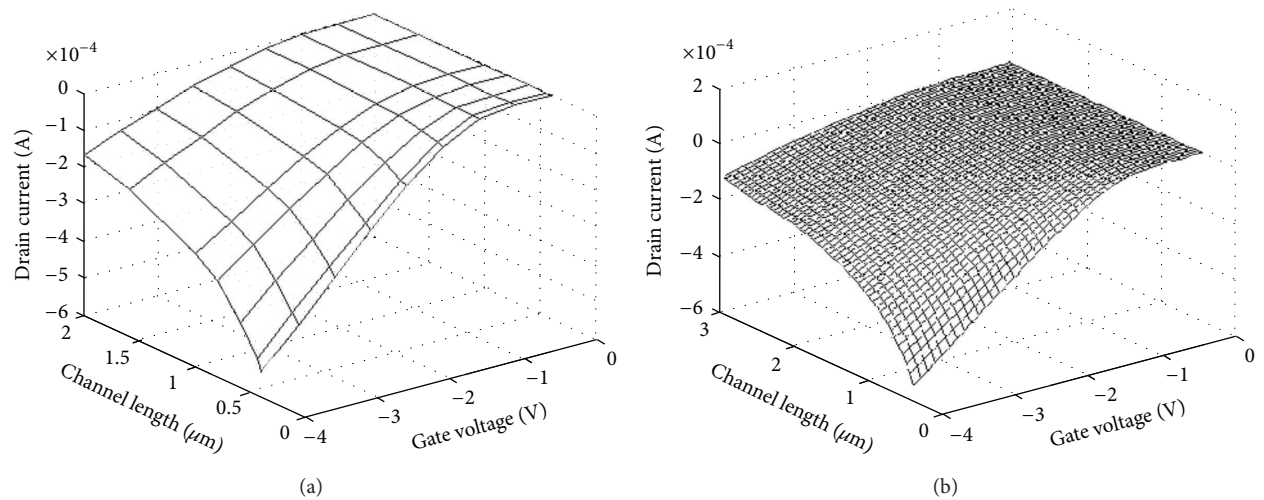


FIGURE 4: The 3D-like I_d (a) measurement data surface and (b) prediction data surface versus L and V_g of the group 1A samples (as $V_d = -3$ V).

percentage of the predicted results was not greater than 0.1% when they were compared with the experimental data.

3.1. For the Group One DUTs. Figures 3(a) and 3(b) are the 3D-like I_d measurement data surface and prediction data

surface versus L and V_d as the gate voltage (V_g) set to be -3 V for group 1A samples ($W = 2 \mu\text{m}$ and L varied). By the same token, Figures 4(a) and 4(b) are the 3D-like I_d measurement data surface and prediction data surface versus L and V_g as the drain voltage (V_d) set to be -3 V for the same group 1A

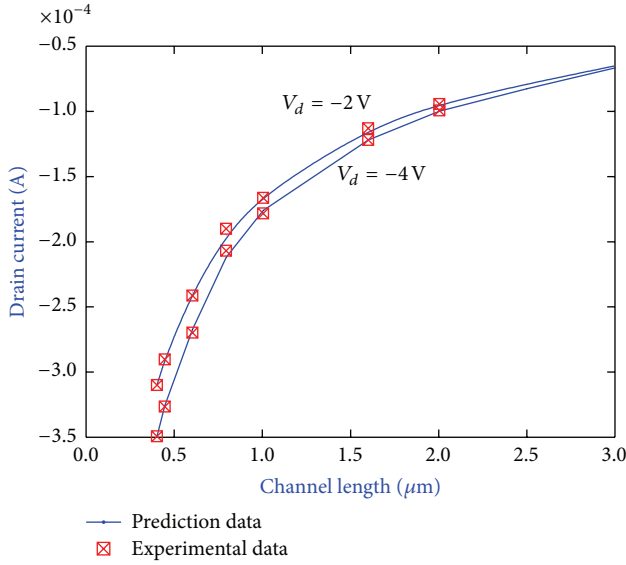


FIGURE 5: Comparison of I_d measured results and training prediction data of the group 1A samples (as $V_d = -2, -4$ V; $V_g = -3$ V).

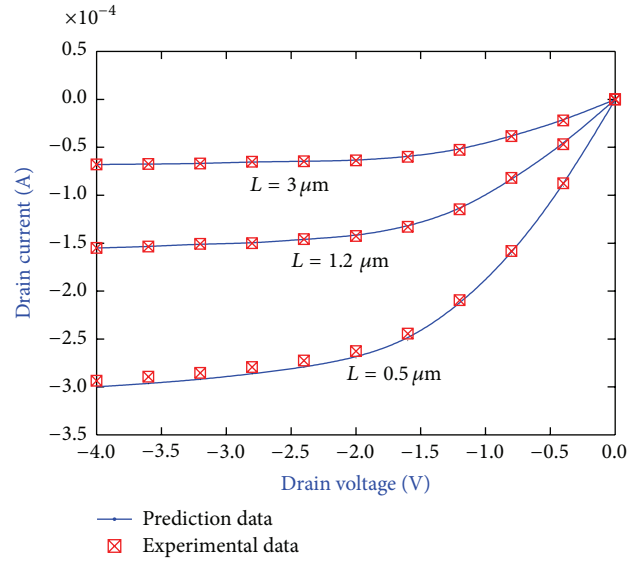


FIGURE 7: Comparison of I_d measured results and prediction data of the group 1B diagnostic samples (as $L = 0.5, 1.2, 3$ μm ; $V_g = -3$ V).

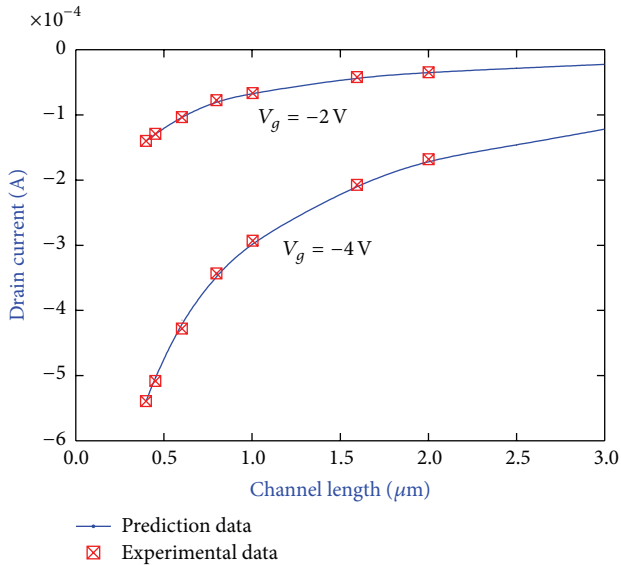


FIGURE 6: Comparison of I_d measured results and training prediction data of the group 1A samples (as $V_g = -2, -4$ V; $V_d = -3$ V).

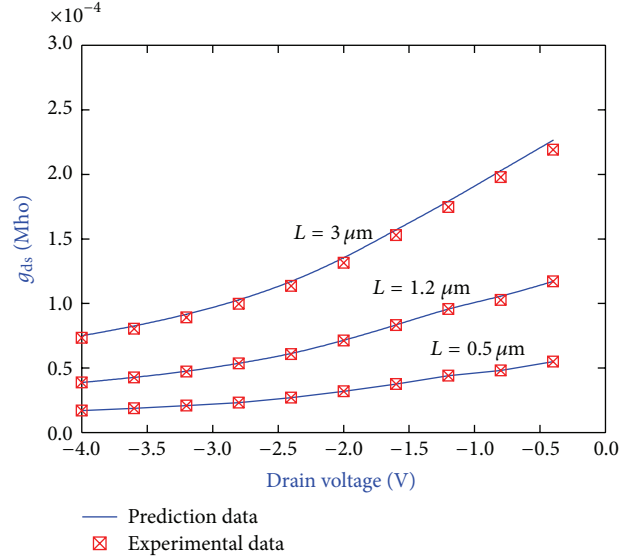


FIGURE 8: Comparison of g_{ds} measured results and prediction data of the group 1B diagnostic samples (as $L = 0.5, 1.2, 3$ μm ; $V_g = -3$ V).

samples. Here, in Figures 3(b) and 4(b), the channel length of the prediction surface was extended to 3 μm . Then, from Figures 3 and 4, for the situations in which $V_d = -2, -4$ V; $V_g = -3$ V and $V_g = -2, -4$ V; $V_d = -3$ V, the good matching I_d results versus channel lengths of group 1A are shown in Figures 5 and 6, respectively. Finally, the comparisons of diagnostic samples (L_3, L_7, L_{10}) of group 1B and the prediction data from Figures 3(b) and 4(b) are shown in Figures 5~9, respectively. Meanwhile herein, for example, the output conductance g_{ds} characteristics versus V_d and L

are also addressed in Figure 8. As shown, highly consistent results were obtained, and the error percentage was no greater than 2.5%.

3.2. For the Group Two DUTs. Figures 10(a) and 10(b) are the 3D-like I_d measurement data surface and prediction data surface versus W and V_d as the gate voltage (V_g) set to be -3 V for group 2A samples ($L = 0.6$ μm and W varied). By the same token, Figures 11(a) and 11(b) are the 3D-like I_d measurement data surface and prediction data surface versus

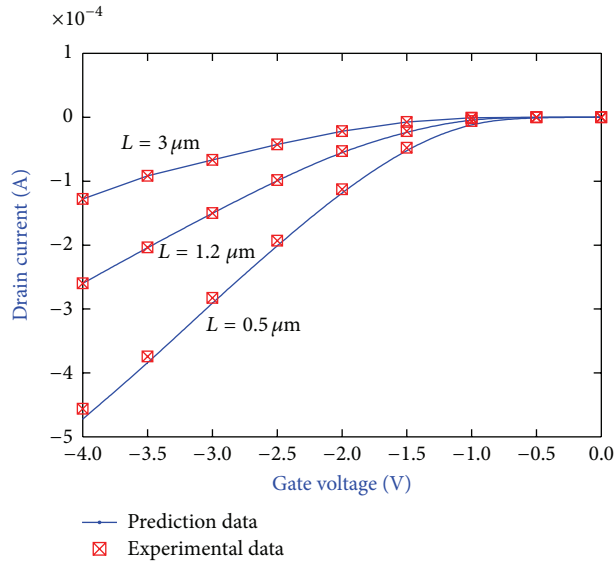


FIGURE 9: Comparison of I_d measured results and prediction data of the group 1B diagnostic samples (as $L = 0.5, 1.2, 3\text{-}\mu\text{m}$; $V_d = -3\text{ V}$).

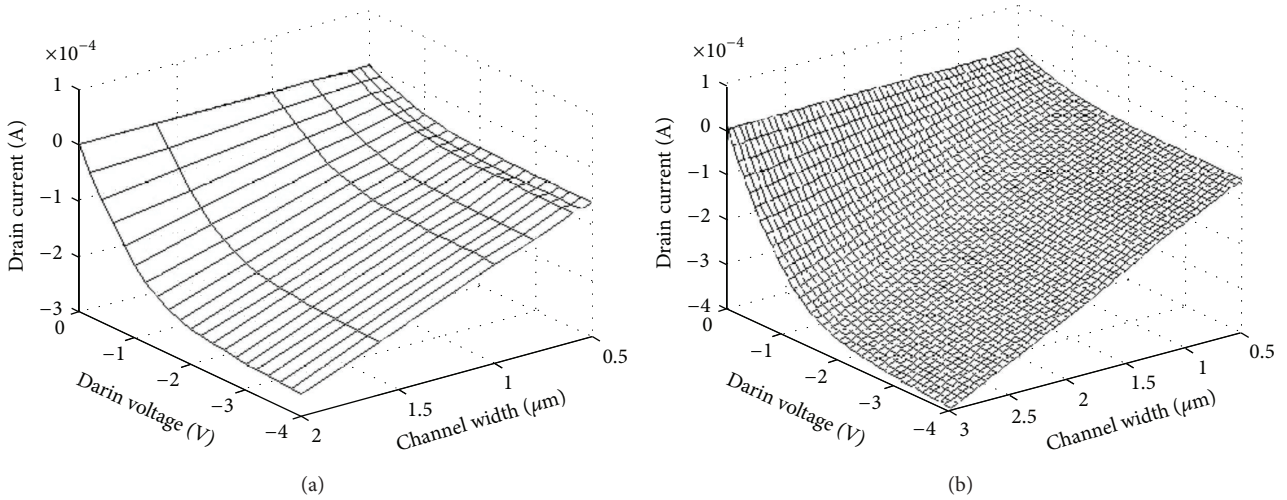


FIGURE 10: The 3D-like I_d (a) measurement data surface and (b) prediction data surface versus W and V_d of the group 2A samples (as $V_g = -3\text{ V}$).

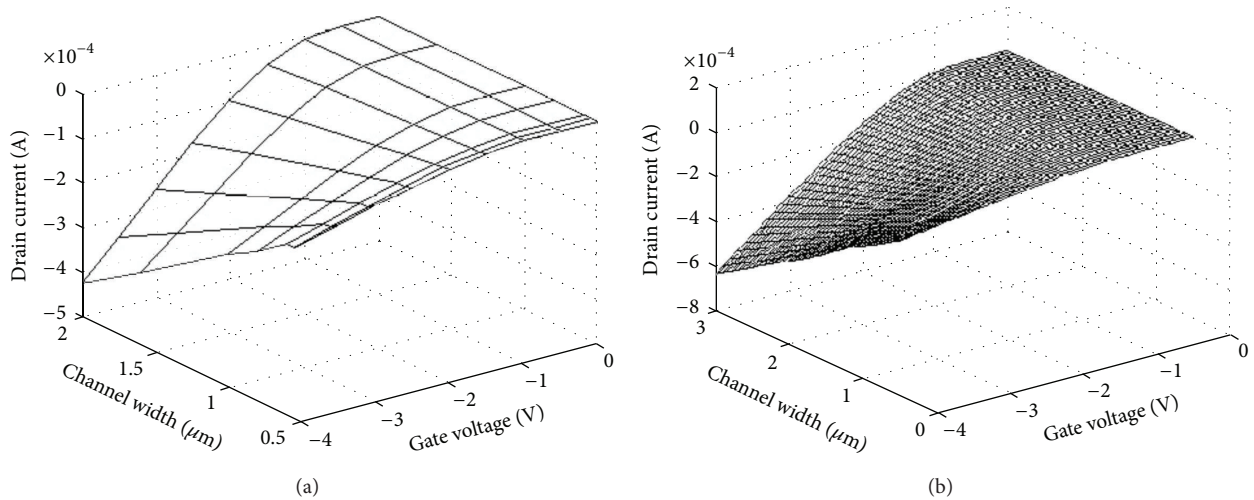


FIGURE 11: The 3D-like I_d (a) measurement data surface and (b) prediction data surface versus W and V_g of the group 2A samples (as $V_d = -3\text{ V}$).

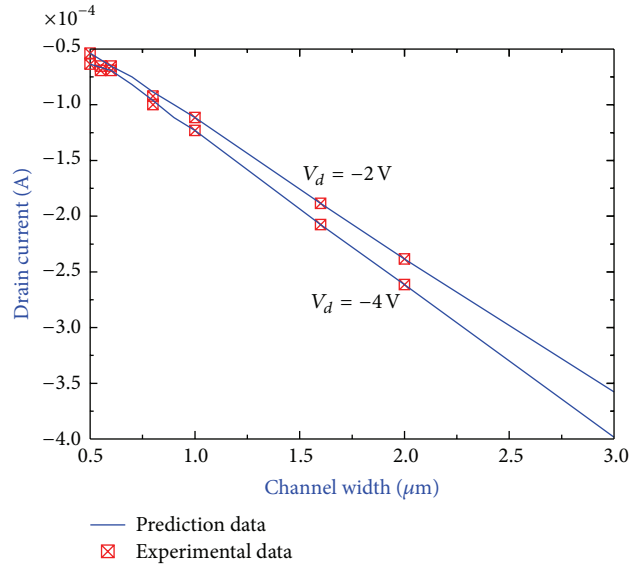


FIGURE 12: Comparison of I_d measured results and prediction data of the group 2A samples (as $V_d = -2, -4\text{ V}$, $V_g = -3\text{ V}$).

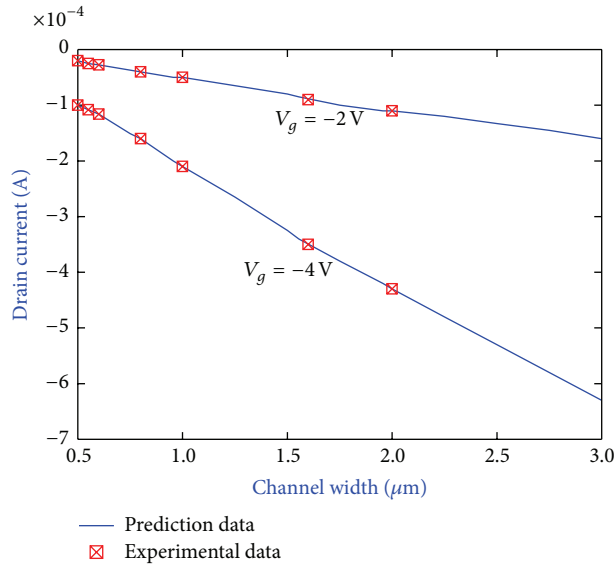


FIGURE 13: Comparison of I_d measured results and prediction data of the group 2A samples (as $V_g = -2, -4\text{ V}$, $V_d = -3\text{ V}$).

W and V_g as the drain voltage (V_d) set to be -3 V for the same group 2A samples. Similarly, in Figures 10(b) and 11(b), the channel width of the prediction surface was extended to $3\ \mu\text{m}$. Then, from Figures 10 and 11, for the situations in which $V_d = -2, -4\text{ V}$; $V_g = -3\text{ V}$ and $V_g = -2, -4\text{ V}$; $V_d = -3\text{ V}$, the good matching I_d results versus channel widths of group 2A are shown in Figures 12 and 13, respectively. Finally, the comparisons of diagnostic samples (W_4, W_7, W_{10}) of group 2B and the prediction data from Figures 10(b) and 11(b) are shown in Figures 14~15, respectively. As shown, highly consistent results were obtained.

4. Conclusion

This paper presents a novel application of ANFIS-based device characteristic prediction that can handle both

geometry dimension and bias voltage inputs. From the above results, it can be seen that there was good agreement between the final prediction data and the measured data of diagnostic DUTs. Thus, it is also shown that the ANFIS can demonstrate the complicated device characterization of a submicron pMOSFET in a highly effective manner. Then, this paper provided a new methodology to predict the complex relation of characteristic behaviors under different geometry dimension of pMOSFET devices. This methodology is excellent for expressing the characteristic behaviors of pMOSFET devices and it can be easily used in complicated submicron devices. Meanwhile, the ANFIS system has the ability to learn quickly and has fast convergence speed, and it does not need to find the transition function or states equation of the prediction system. Therefore, all

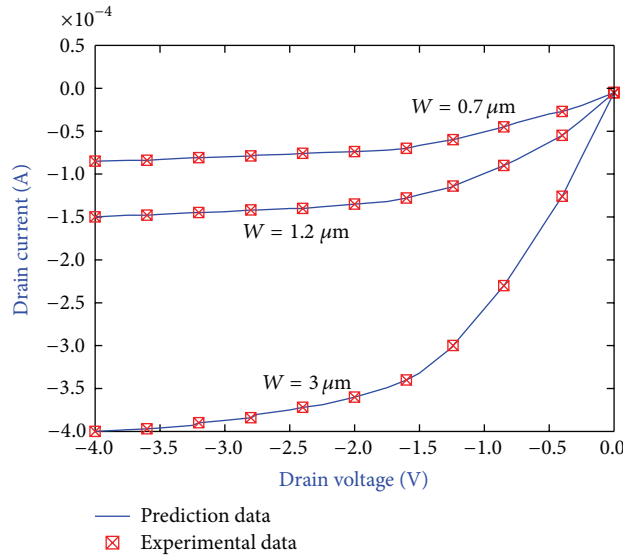


FIGURE 14: Comparison of I_d measured results and prediction data of the group 2B diagnostic samples (as $W = 0.7, 1.2, 3\text{-}\mu\text{m}$, $V_g = -3\text{ V}$).

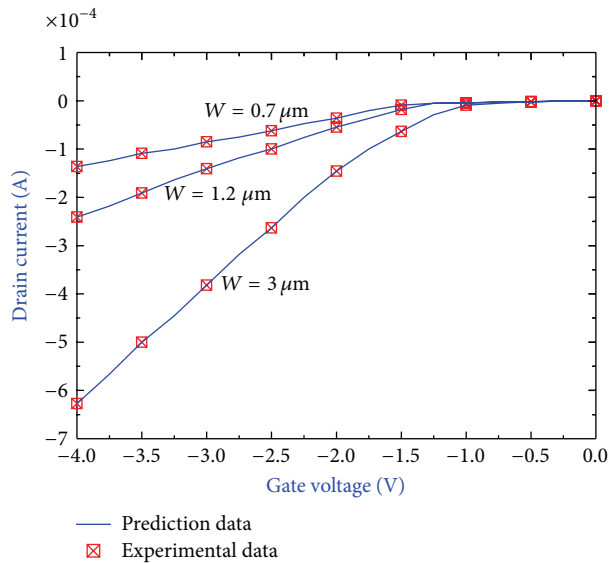


FIGURE 15: Comparison of I_d measured results and prediction data of the group 2B diagnostic samples (as $W = 0.7, 1.2, 3\text{-}\mu\text{m}$, $V_d = -3\text{ V}$).

the measured data can be treated as the training data in ANFIS. Furthermore, this novel technique does not require any assumed parameters, so the same procedure could easily be applied to analyze or predict other complicated physical behaviors in ULSI simulations.

Conflict of Interests

The author confirms that there is no conflict of interests regarding the publication of this paper.

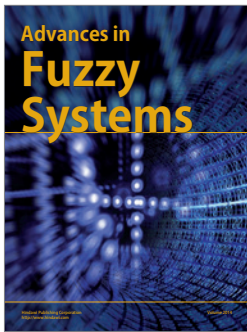
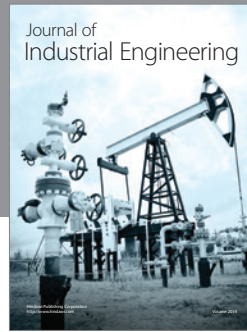
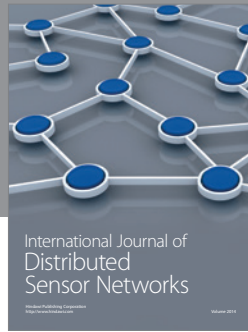
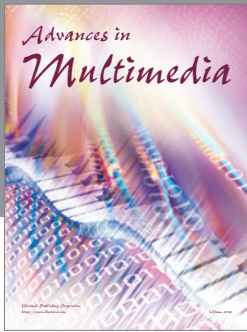
Acknowledgment

In this work, author would like to thank the National Chip Implementation Center in Taiwan for providing the process information and fabrication platform.

References

[1] S. S.-S. Chung, T.-S. Lin, and Y.-G. Chen, “An efficient semi-empirical model of the I-V characteristics for LDD MOSFETS,”

- IEEE Transactions on Electron Devices*, vol. 36, no. 9, pp. 1691–1702, 1989.
- [2] M. A. Imam, M. A. Osman, and A. A. Osman, “MOSFET global modeling for deep submicron devices with a modified BSIM1 SPICE model,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 15, no. 4, pp. 446–451, 1996.
 - [3] H. T. Mebrahtu, W. Gao, W. E. Kieser, X. L. Zhao, P. J. Thomas, and R. I. Hornsey, “SPICE models of fluorine-ion-irradiated CMOS devices,” *IEEE Transactions on Electron Devices*, vol. 54, no. 8, pp. 1963–1971, 2007.
 - [4] Y. Qiang Li, T. Krakowski, P. Francis, and L. Smith, “Scalable spice modeling of integrated power LDMOS device using a cell-based building block approach,” in *Proceedings of the 20th International Symposium on Power Semiconductor Devices and IC’s (ISPSD ’08)*, pp. 88–90, Orlando, Fla, USA, May 2008.
 - [5] C. Yakopcic, T. M. Taha, G. Subramanyam, and R. E. Pino, “Generalized memristive device SPICE model and its application in circuit design,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 32, no. 8, pp. 1201–1214, 2013.
 - [6] A. Ruangphanit, N. Sakuna, B. Niemcharoen, and R. Muangh-lua, “Implementation of the temperature and narrow channel dependence on threshold voltage model of NMOSFETs,” in *Proceedings of the 4th Joint International Conference on Information and Communication Technology, Electronic and Electrical Engineering*, pp. 1–4, 2014.
 - [7] B. J. Sheu, D. L. Scharfetter, P.-K. Ko, and M.-C. Jeng, “BSIM: Berkeley short-channel IGFET model for MOS transistors,” *IEEE Journal of Solid-State Circuits*, vol. 22, no. 4, pp. 558–566, 1987.
 - [8] T. Kim, N. Franklin, C. Srinivasan, P. Kalavade, and A. Goda, “Extreme short-channel effect on RTS and inverse scaling behavior: source-drain implantation effect in 25-nm NAND flash memory,” *IEEE Electron Device Letters*, vol. 32, no. 9, pp. 1185–1187, 2011.
 - [9] A. Valletta, L. Mariucci, A. Pecora, L. Maiolo, S. D. Brotherton, and G. Fortunato, “Analysis of kink effect and short channel effects in fully self-aligned gate overlapped lightly doped drain polysilicon TFTs,” *Journal of Display Technology*, vol. 9, no. 9, pp. 764–769, 2013.
 - [10] G. Fuse, M. Fukumoto, A. Shinohara, S. Odanaka, M. Sasago, and T. Ohzone, “A new isolation method with boron-implanted sidewalls for controlling narrow-width effect,” *IEEE Transactions on Electron Devices*, vol. 34, no. 2, pp. 356–360, 1987.
 - [11] K.-L. Yeh and J.-C. Guo, “Narrow-width effect on high-frequency performance and RF noise of sub-40-nm multifinger nMOSFETs and pMOSFETs,” *IEEE Transactions on Electron Devices*, vol. 60, no. 1, pp. 109–116, 2013.
 - [12] C.-Y. Lu and J. M. Sung, “Reverse short-channel effects on threshold voltage in submicrometer Salicide devices,” *IEEE Electron Device Letters*, vol. 10, no. 10, pp. 446–448, 1989.
 - [13] Q. Xie, C.-J. Lee, J. Xu, C. Wann, J. Y.-C. Sun, and Y. Taur, “Comprehensive analysis of short-channel effects in ultrathin SOI MOSFETs,” *IEEE Transactions on Electron Devices*, vol. 60, no. 6, pp. 1814–1819, 2013.
 - [14] J. Zhou, S. Jayapal, J. Stuyt, J. Huisken, and H. De Groot, “The impact of inverse narrow width effect on sub-threshold device sizing,” in *Proceedings of the 16th Asia and South Pacific Design Automation Conference*, pp. 267–272, January 2011.
 - [15] S. Pandit and C. K. Sarkar, “Modeling the effect of gate fringing and dopant redistribution on the inverse narrow width effect of narrow channel shallow trench isolated MOSFETs,” in *Proceedings of the 24th International Conference on VLSI Design*, pp. 195–200, January 2011.
 - [16] J. Zhou, M. Cheng, and L. Forbes, “SPICE models for flicker noise in p-MOSFETs in the saturation region,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 20, no. 6, pp. 763–767, 2001.
 - [17] W. Liu, “Appendix A: BSIM3 equations,” in *MOSFET Models for SPICE Simulation: Including BSIM3v3 and BSIM4*, pp. 473–506, WILEY-IEEE Press, 2001.
 - [18] Y. Singh Chauhan, S. Venugopalan, N. Paydavosi et al., “BSIM compact MOSFET models for SPICE simulation,” in *Proceedings of the 20th International Conference on Mixed Design of Integrated Circuits and Systems, MIXDES 2013*, pp. 23–28, June 2013.
 - [19] M. A. Shoorehdeli, M. Teshnehlab, and A. K. Sedigh, “A novel training algorithm in ANFIS structure,” in *Proceedings of the American Control Conference*, pp. 5059–5064, June 2006.
 - [20] S. P. Srinivasan and P. Malliga, “A new approach of adaptive Neuro Fuzzy Inference System (ANFIS) modeling for yield prediction in the supply chain of Jatropa,” in *Proceedings of the IEEE 17th International Conference on Industrial Engineering and Engineering Management*, pp. 1249–1253, Xiamen, China, 2010.
 - [21] A. Al-Hmouz, J. Shen, R. Al-Hmouz, and J. Yan, “Modeling and simulation of an Adaptive Neuro-Fuzzy Inference System (ANFIS) for mobile learning,” *IEEE Transactions on Learning Technologies*, vol. 5, no. 3, pp. 226–237, 2012.
 - [22] A. S. M. Jaya, S. Z. M. Hashim, H. Haron, R. Ngah, M. R. Muhamad, and M. N. A. Rahman, “Modeling of ANFIS in predicting TiN coatings roughness,” in *Proceedings of the 5th International Conference on Computer Science and Information Technology (CSIT ’13)*, pp. 13–18, March 2013.
 - [23] W. Li, P. Wang, and Y. Li, “A method of adaptive colored noise cancellation based on ANFIS,” in *Proceedings of the International Conference on Image Analysis and Signal Processing*, pp. 386–388, Linhai, China, April 2009.
 - [24] N.-N. Yan, Z.-C. Fu, and Q. Zhou, “ANFIS approach for noise reduction of lightning current online monitoring system,” in *Proceedings of the 7th Asia-Pacific International Conference on Lightning (APL ’11)*, pp. 618–624, November 2011.
 - [25] M. Sharique and M. A. Ali, “Two step impulse noise suppression in greyscale images using ANFIS,” in *Proceedings of the International Conference on Multimedia, Signal Processing and Communication Technologies*, pp. 80–83, 2013.
 - [26] S. Anissa, S. Hassene, and B. B. Ezzedine, “Adaptive median filter based on ANFIS for impulse noise suppression,” in *Proceedings of the IEEE 23rd International Symposium on Industrial Electronics (ISIE ’14)*, pp. 950–953, Istanbul, Turkey, June 2014.
 - [27] S. Rojathai and M. Venkatesulu, “Noise robust tamil speech word recognition system by means of PAC features with ANFIS,” in *Proceedings of the 13th IEEE/ACIS International Conference on Computer and Information Science*, pp. 435–440, Taiyuan, China, June 2014.



Hindawi

Submit your manuscripts at
<http://www.hindawi.com>

